Interview with Hugo Pristauz from Datacon

Datacon, headquartered in Radfeld, Austria was founded in 1986 and is now part of the Dutch Besi group. Datacon's main area of expertise is the development and production of high-precision flip chip and die bonding equipment for the microelectronics industry. Dr Hugo Pristauz, VP of Besi flip chip division has agreed to be interviewed for 3D Packaging.

Dr Hugo Pristauz, VP of Besi flip chip division, Datacon

Yole Développement: Before we begin how about a little information on your background before Datacon?

Hugo Pristauz: I studied electrical engineering at the Technical University in Graz with a focus on control engineering receiving a PhD degree in control science. After 8 years teaching at the university I spent 4 years as R&D manager in an automation company.

YD: Dr. Pristauz, we have heard that many people around the world call you Dr. Flip Chip – what's the story behind that?

HP: Well, my whole life in semiconductor business was dealing with flip chip, and especially in Asia my family name is hard to remember – it's the same difficulty for me to keep Chinese names in mind. So I always offer the people I'm meeting to call me just "Hugo" or "Dr. Hugo" or even "Dr. Flip Chip" if they feel more comfortable. And people are amused by this offer, but it works reliably: They always remember me by at least one of these offered names.

YD: And what are your responsibilities at Datacon?

HP: I started at Datacon in 1999 as manager of the newly installed Advanced Technology department. From that time I have been continually involved in the development of different branches of flip chip technologies. Two years later I received the opportunity to develop Datacon's flip chip business and was also in charge of the development of our 8800 high speed flip chip platform, which is now an important part of Besi's product portfolio. Currently I am VP of Besi flip chip division which comprises both Datacon and Esec flip chip solutions.

YD: In chip movement there is always a tradeoff between speed and accuracy. Can you describe what these bounds are for Datacon tools?

HP: I absolutely agree with you that these two requirements are key for any flip chip tool. But there is a third requirement which is big working area. Developing a flip chip machine which can do its job with high accuracy and excellent speed on a big working area is a technical challenge. With Datacon's 15 year strategic focus on flip chip our engineers have had time to develop machine technologies to meet these highly flexible and productive flip chip targets. Our 8800 technology powers our leading market position in flip chip equipment.

YD: Thin die appears to be a generic trend no matter what the packaging type. What is Datacon's perspective on how thin a die can get and still be handled by your equipment ? What changes are needed to the toolset and at what thickness ? Is there a known relationship between the amount of pressure that can be applied to the thinned die once it is placed and the accuracy of placement? For instance, if I am moving a 5mm 50µm thick die for 3DIC stacking with Cu/Sn interconnect how much pressure can I put on the die once placed?

HP: Good question. Well, the roadmaps for thin FC are targeting 50µm in the next few years and 40µm in the future. For standard die bonding (non flipped) 30µm thick die are running in mass production on Besi equipment. A basic principle is that thin flip chip bonding has almost nothing to do with thin standard die bonding. First of all, bumped dies are more stress sensitive compared to non bumped die. Also, handling of bumped dies (if vacuum tools are touching bumped die surface) is different from handling non-bumped dies. And finally after leaving the die on the substrate additional issues can arise when the die warps (e.g. wetting issues). These challenges call for a complete new flip chip bonding method as it is approached by the thermo-compression / local reflow method.

I would say the pressure itself is an almost meaningless quantity since it depends very much on the pressure in combination with some other factors (bending stress of chip during ejection, support of chip during handling, choice of bonding process, etc.).

YD: Same question for die size. What is the largest die that can currently be handled and, more importantly what is the smallest (x,y size) die that can be moved?

HP: We offer solutions for 50 x 50mm flip chips, but real demands for big flip chip are 25 x 25mm to 30 x 30mm in the field of TSV silicon interposers. At the other end of the scale 0.4 x 0.4mm flip chips are running in high volume applications on our RFID assembly lines, while our standard spec goes down to 0.3 x 0.3mm. Currently we are working on rectangular flipped dies where one edge is less than 0.1mm. Since our machines are both preferred in high volume production but also in R&D labs we have to support a big die size spectrum.

YD: In the early 1990's there was a trend towards direct chip attach (DCA) by using interconnects such as WB, TAB and FC directly on substrate (chip-on-board, chip-on-flex-chip-on-glass etc) . Are you seeing much of that now ? – has it given way to WLP or is that really only a matter of semantics at this point?

HP: Still in the year 2000 these applications have been figured out to possess high growth potential. Fact is that these applications have very limited meaning which is very much depending on the boundary conditions. And there is a simple reason: typically the substrate for a high bump count flip chip is very expensive because of the required wiring density. But this wiring density is typically not needed on standard board level for interconnecting the SMT components. If you decide for DCA FC you usually gain some minor advantages (cost, form factor) by eliminating the package with the big trade-off of increased substrate costs on an area which might be hundred times bigger than a flip chip interposer area is. This is why there are currently only limited requests for FC DCA. If, however, the bump pitch is moderate, then the previously mentioned argument does not hold anymore. This is the case for RFID (which is a chip on flex application) where both volume and growth potential is big.

YD: What other trends have you seen developing over the years in the flip chip (FC) market.

HP: After 10 years of almost steady technology in the flip chip mainstream we are entering now "The New World of Flip Chip". First of all the major technology was with C4 type bump technology (controlled collapse chip connection – IBM terminology). Due to the collapse of the bumps there is a lower limitation in pitch which is usually around 130µm. A proper machine accuracy to handle this pitch is 10-12µm accuracy (In Datacon language all accuracy specs relate to 3 sigma). Below this bump pitch the capillary underfill process (CUF - which is a quasi standard for these applications) will generate issues due to the small gap between chip and bonder.

To overcome this road block, a new flip chip technology based on non-collapsing copper pillar bumps has been developed and deployed. Based on this C2 technology (C2 = chip connection – IBM terminology) which, like C4, is still achieved with a subsequent mass reflow high volume production of 70µm bump pitch is already in place and people are not scared to progress to C2-based 60µm pitch target. For this new C2 technology we have 6µm machines in our portfolio. But these are still not the cutting-edge requirements: driven majorly by smart phone and smart tab applications new IC standards are expected by 2013 (wide I/O interface, low power consumption ICs). The targeted bump pitches to achieve these requirements are down to 40µm with 3µm accuracy for the flip chip bonder.

But improvement of the accuracy is not the whole story. As the die thickness has also to be decreased accordingly the current two-step process (flip chip bonding, subsequent mass reflow) it has to be replaced by a one-step bonding process which is commonly known under thermo compression / local reflow which requires a couple of new capabilities in the bonder. This process seems also to be the favorite flip chip process for TSV chip-to-wafer applications. In parallel, new flip chip opportunities have opened up in LED, CIS (CMOS image sensors) and MEMS applications where GGI (gold gold interconnect) based on ultrasonic/thermosonic bonding have proven to have a lot of advantages.

YD: What is your perspective on the percentage of dies that are now being interconnected by FC?

HP: Regarding the share of flip chip applications there are several numbers published by marketing institutes. Besi made about 15% of its "die attach" revenue in 2010 with flip chip equipment which shows that flip chip technology has already reached significant growth.

YD: Underfill is another technology that has changed a lot over the last 20 years. Can you comment on what Datacon has seen here?

HP: As I mentioned CUF (post-applied capillary underfill) is getting challenging with shrinking bump pitch. While pre-applied underfill is a standard in RFID applications it will now also come as a standard in combination with thermo compression / local reflow, since the underfill process cannot be separated anymore from the pure bonding step. But there is a quite different driver for changing the underfill process also for bigger bump pitch. Driven by cost-reduction a new technology MUF (molded underfill) has both resulted in lower assembly costs and simplification of the process. Here our molding solutions from Besi/Fico are quite impressive.

YD: What makes your FC equipment stand out vs competitors?

HP: Maturity, maturity, maturity. And finally our capability to support our customers with flip chip process know-how. It is quite amazing how many customers select our flip chip equipment without making use of a second source. If you consider, however, that a flip chip bonder software comprises

High precision flip-chip bonder (Courtesy of Datacon) more than 1.5 Mio lines of source code and that about 90% of the software are made for easy-to-use and resume handling (smooth recovery from error states) then you might get an impression how many engineering hours have been invested to result now in perfect flip chip equipment. In my opinion the decisions of our customers are mainly based on risk minimization. Especially in the world of high competition, the risk of lacking yield but also the risk of lacking uptime can jeopardize the business seriously. Flip chip products are high margin products and quality can never be compromised. And it needs to be understood: flip chip is still an emerging technology. The better the equipment capabilities are and the higher the flexibility of the tool is, the lower the risk is of failing the targets in an emerging world. And that are exactly the added values we can provide to our customers with our excellent flip chip tools.

YD: 3D IC is a very active technology right now. Can we get your general comments on what Datacon is seeing here ? (1) C2W vs W2W; (2) thickness of the layers; (3) bonding techniques being used?
HP: In fact this is a topic which is important for the future, and if I mention 'future' I mean that it will not be in mass production in soon. Anyway if you understand the technical requirements then this technology will come. First of all we see that C2W (chip to wafer) is a must in the major field of 3D integration (3DI), and this 'must' comes from the yield requirements. Second all the capabilities which we have developed for the 40µm pitch applications in connection with thin die handling and the thermocompression / local reflow process is also the right process for 3DI/C2W. In addition we are optimizing our alternative process flow which we call AC2W (advanced chip to wafer) for 3DI.

YD: Datacon is also known for having strong solutions for FO-WLP?
HP: Definitely FO-WLP (Fan-out wafer level packaging, sometimes better known as eWLB – Infineon terminology) was one of the best opportunities we had in the past two years. As I mentioned C2W applications are rarely in mass production, but for eWLB we had the excellent opportunity to provide a big bunch of equipments for the mass production. Exactly speaking eWLB is not really chip-to-wafer but for the flip chip bonder the challenge is very similar. The required 10µm "global accuracy" on a 12" wafer level area is comparable with a 6µm "local accuracy" on the same area. The big installed base of eWLB bonders (100% market share) gives us a good feedback of the maturity of the 6µm accuracy option on our 8800 platform we launched recently.

YD: Datacon appears to be a major player in European R&D programs [Hydromel, DAVID, Hiding Dies, FLIBUSI, 3DICE] Can you update us on the status of some of these programs and what is coming up on the R&D front in the future?
HP: For confidentiality reasons I cannot give any details on those projects beyond the information which has been already published. I'd like to thank the Austrian government and the European Community which have funded us in the above mentioned projects. While we are doing R&D on the emerging "New World of Flip Chip" technologies listed above, Datacon remains fully focused on developing robust equipments for the industry short term needs which meet our customers expectations regarding ease of use and uptime "without headaches".

www.datacon.at