

## INTERVIEW

## Exclusive interview with Markus Wimplinger – EV Group



At the recent SEMICON West event in San Francisco, Yole Developpement was able to sit down with EV Group's Markus Wimplinger, Corporate Technology Development & IP Director, about the global status of 3D IC.

**Yole Developpement:** What can you tell us about EVG 300-mm tools that have been placed in global consortia and or major global 3D players?

**Markus Wimplinger:** We currently have 300-mm tools placed at Leti, Fraunhofer IZM-Dresden, IME and Sematech. We also have 200-mm tools at IMEC, IME, Fraunhofer IZM Berlin, as well as LETI. We also have activities with a number of major OSATs. Amkor has stated previously in public that they have our tools installed in the area of temporary bonding and debonding for thin wafer handling. A major IDM, who I cannot name, has installed both 200- and 300-mm bond/debond tools and of course we all know about the only current commercial 300-mm 3D IC line, which is in production for CMOS image sensors (CIS) at ST Micro who are using our tools.

**YD:** Lets talk about W2W and D2W bonding. The industry seems to have swung to D2W in the last few years. What are you seeing in the field?

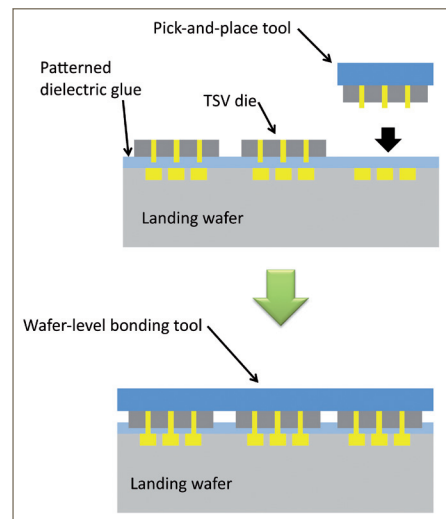
**MW:** We see both W2W and D2W eventually having segments in the market. Our current capability for W2W alignment is  $0.5 \mu\text{m } 3 \sigma$  (post-bond) which has recently been verified by the Sematech group. Versus 12 months ago, when nearly all our customers wanted D2W, we have seen some shift back to W2W bonding recently.

In D2W bonding, known-good-dies (KGDs) are attached to the good dies in the bottom device wafer. Such chip-to-wafer bonding through metal-metal thermo-compression mechanisms, such as CuSn intermetallic bonding or Cu-polymer hybrid bonding, is expected to be used for future TSV applications.

With these bonding methods, where the metal inter-diffusion is proportional to temperature, pressure and time, it is not economically feasible to perform the bonding process at a single-die level. The basic idea behind the EV Group "Advanced Chip-to-Wafer" (AC2W) bonding is to split the bonding process into two sub-steps. The temporary pre-bonding with alignment is performed on a pick-and-place tool, whereas the permanent bonding of KGDs is performed as a batch process in a dedicated EV Group's AC2W bond chamber.

The permanent bonding process requires a controlled, homogeneous, perpendicular force to be applied on every single chip due to non-uniform

distribution of KGDs on the base device wafer. A non-uniform KGD distribution can result in a possible shift in the center of gravity away from the actual center of the bottom substrate. This occurrence requires a controlled shift in the center of applied force during the bonding process in a chamber. A true KGD stacking can be achieved through the control of the center position and the direction of the applied force.



D2W process flow for 3DIC integration  
(Courtesy of EVGroup)

Direct die-to-wafer throughput can be optimized for 3D TSVs with this two-step process. The TSV dice are aligned and placed onto the landing wafer using a pick-and-place tool (top). The fully populated wafer is then moved to a wafer-level bonding tool where pressure and heat are applied simultaneously to all stack dice.

**YD:** In terms of metal – metal bonding technology, what do you see as the most popular choices at the OSATs right now and why?

**MW:** At  $40 - 50 \mu\text{m}$  pitch they will probably use C4 since they already have this technology in house and they are very comfortable with it. For more advanced pitch requirements, we see significant interest in Cu/Sn IMC technology. This metallization, however, is new for traditional OSATs and hence, requires more efforts on qualification. In the long run, at  $200$  to  $300^\circ\text{C}$ , Cu-Cu is probably the best technical solution, but the OSATs have the least experience here and they are fearful of the throughput limitations. Also, significant further development will be needed to enable Cu-Cu bonding reliably and repeatable at those temperatures.

**YD:** Many of the recent roadmaps from foundries such as TSMC and OSATs such as Amkor and ASE are pointing towards 2011-2012 for 3D IC commercial production. Do you see these roadmaps as aggressive or realistic?

**MW:** I think 2012 seems realistic for those who have been working in the area for the last few years. Not all, but some significant numbers of players will be ready in 2012. A majority of them will be in Asia.

**YD:** Are there any qualified 3D IC lines in place yet? What do you see as the likely timing here? Why have we not seen process ground rules coming out of foundries or IDMs yet?

**MW:** As I said earlier, the ST Micro line that is producing commercial quantities of CIS die is fully qualified and in production.

Many customers are working on qualifying their lines as we speak and some are scheduled to be done in 4Q 2010. They do have ground rules ready. One can assume that ground rules for their processes have been released to key customers (2-3 max).

Most serious players are taking the pragmatic approach of "lets use what we have now knowing that the technology will develop as we go forward."

**YD:** Markus, anything else you'd like to add?

**MW:** EV Group has been focused on TSV and 3D during the recent economic downturn and it has done very well for us. We continue to see this as a major thrust of our business and will be continuing our joint work with customers and partners in this highly active area.

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**Markus Wimplinger**  
Corporate Technology  
Development & IP Director

Markus Wimplinger oversees EV Group's global process engineering team and

manages R&D partnerships, third-party contracts and IP affairs. Prior to this role, he served as director of technology with EV Group North America in Tempe, Ariz. Mr. Wimplinger joined EVG in 2001 as a project manager.