

Next Generation Package Substrates: 3D silicon and glass Interposers

Technologies, applications and markets

August 2010 – Report sample

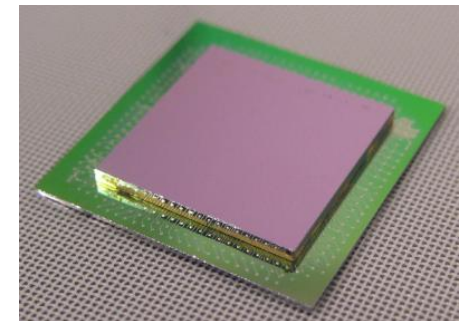
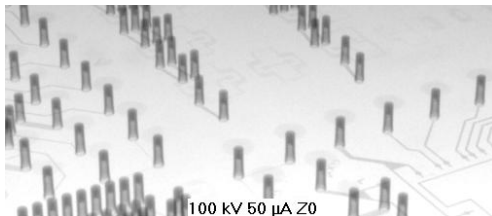
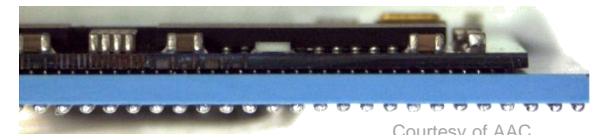
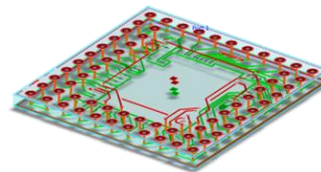
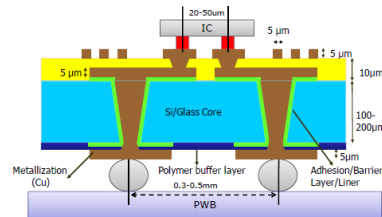
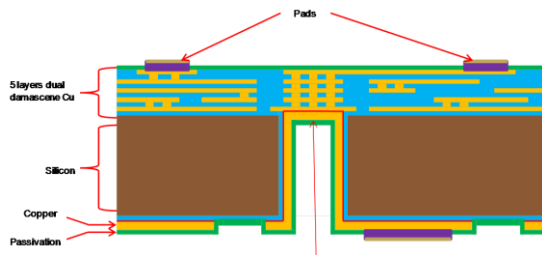
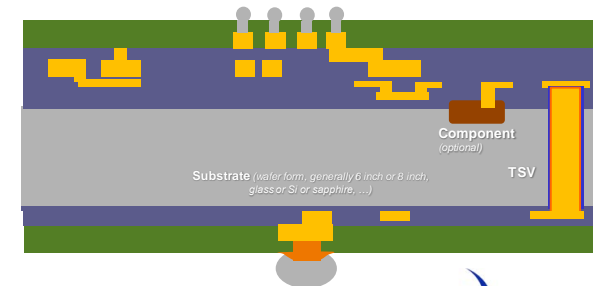


Table of contents

1. Scope of the report & definitions	2	5. Competing solutions and technologies by application segment	178
2. Executive summary	21	6. Cost	189
3. Applications and drivers	40	– Cost structure of silicon interposers and influential parameters	
1. Interposers for MEMS & sensors	45	– Acceptable « prices », cost targets	
2. Logic interposers	52	– Cost down roadmaps	
3. Logic + memory interposers	69	– Case examples	
4. Interposers for CMOS image sensors	80	7. Supply chain analysis	206
5. 3D silicon submounts for HB LEDs	90	– Critical review of the likely interposer manufacturers and supply chain organization by application segment	
6. 3D Power/Rf/analogue integrated passives	99	– Declared or visible players and their respective positions	
7. Interposers for memory stacks	108	8. Market forecasts	220
8. Misc. Glass/silicon package substrates	114	– 2009-2015 market forecasts In M\$ by application, substrate material size and shape	
4. Technologies of 3D silicon/glass interposers	130	– 2009-2015 wafer forecasts in kWafers (wspy) by application, substrate material size and shape	
– Substrate materials, substrate thickness, routing metal, routing layers, dielectrics, patterning method, via drilling and filling, wafer and panel sizes	132	9. Roadmaps	227
– Technology preferences by application	166	10. Conclusions	234
– Design rules	179		



This is the first ever report dedicated to 3D (si/glass) interposers

Why this report ? (1)

- **Semiconductor packaging has evolved considerably for the past 10 years, motivated by:**
 - The continuous need for system miniaturization
 - The continuation of Moore's law and the growing gap between silicon fine geometries and packaging substrates' relative coarse definitions
 - The continuously increasing gap between printed circuit boards and integrated circuits, both in terms of geometries and materials
- **As a consequence, System-in-Package (SiP), Package-on-package (PoP), flip-chip Ball grid Array (fc-BGA) or wafer-level packaging (WLP) techniques developed and considerably grew in the past years. WLP uses (usually partly amortized) silicon wafer fab equipments and techniques (photolithography) and allows for**
 - Chip-scale packaging and very high routing densities
- **More recently, the emergence of through silicon vias introduced the possibility to extend the capabilities of silicon/glass interposers to the 3rd dimension**
- **As a consequence, the so-called mid-end infrastructure consisting in foundries for wafer-level packaging operations have developed at an unprecedented pace over the past 3 years to meet the growing demand for Wafer-Level Chip-Scale Packaging (or "fan-in WLCSP") and flip-chip. These new facilities, half way between front-end foundries and regular assembly and packaging facilities, now support high volume manufacturing on large size wafers, thus permitting economies of scale.**
- **3D (silicon or glass) interposers combine wafer-level techniques and advantages with 3D routing capabilities. They now enter the competitive arena of package substrates and propose new growth opportunities for the now established mid-end infrastructure.**

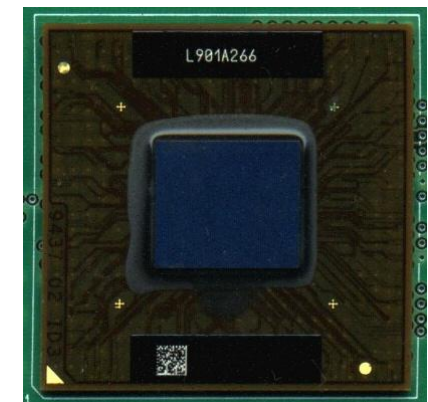
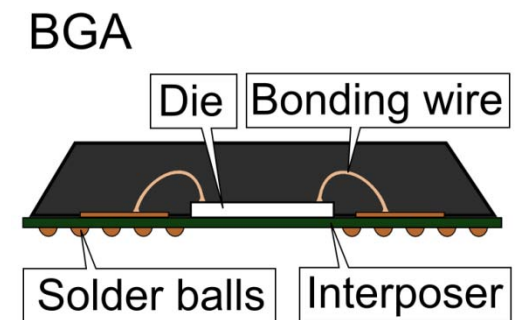
This is the first ever report dedicated to 3D (si/glass) interposers

Why this report ? (2)

- **However, it is not clear yet for the industry what the sweet spots for these 3D interposers will be**
 - for which applications?
 - Will the acceptable price exceed the manufacturing cost?
 - Will it be an intermediate step to 3D TSV's in active IC's, or is it a long term trend?
 - How will the supply chain evolve to serve this emerging market?
 - What will be the market size in the coming years?
 - Indeed, whereas this seems a very attractive market with looming ahead opportunities, and as we were compiling the data for this report, Sixis, a wholly-dedicated company to silicon interposers, was declared insolvent, shedding a different light on this emerging trend of the semiconductor packaging industry.
- **These are the questions we address in this first-ever dedicated report on 3D glass/interposers.**
- **In the report, we list all the 3D interposer opportunities by application, and we analyze the drivers and expected benefits, as well as the alternative options. We make the case for some realistic interposer technology options by comparing their expected costs to acceptable market prices. We list some industry players involved in the 3D interposers field and we synthesize what we clearly see as the latest supply chain related moves. Finally, we propose a market roadmap and associated forecasts.**

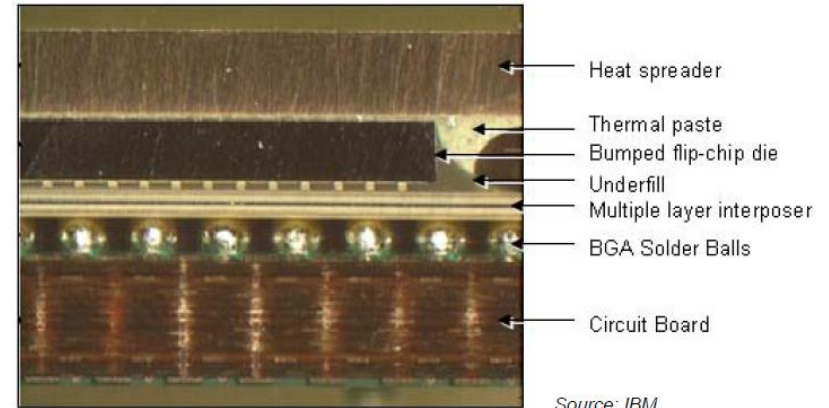
Definitions of « interposer »

- **1994 National Technology Roadmap for Semiconductors :**
an electrical interconnection structure used between a silicon integrated circuit die and package, test jig, or other die that enables a reduced contact pad pitch on the die.
- **Wikipedia:** An interposer is an electrical interface routing between one socket or connection to another. The purpose of an interposer is to spread a connection to a wider pitch or to reroute a connection to a different connection. Interposer comes from the Latin, *interpōnere*, meaning '*to put between.*' [\[2\]](#)
 - A common example of an interposer is an integrated circuit die to BGA, such as in the Pentium II. This is done through various substrates, both rigid and flexible, most commonly FR4 for rigid, and polyimide for flexible. [\[1\]](#)



Our definition of 3D silicon/glass interposers

- There is no normed definition as of today
- Our definition
 - A 3D silicon/glass interposer is an interposer (see definitions on previous slide) which is
 - Made of silicon or glass
 - Equipped with vertical through via electrical connections
 - Patterned by photolithography
- Synonyms
 - Silicon/glass carriers, substrates
- Different types of silicon/glass 3D interposers
 - 3D Silicon/glass interposers may embed various built-in components:
 - Passive components, zener diodes, some transistors (level shifting, buffering).
 - We will need in the future to set a scope definition boundary between 3D integrated circuits and 3D silicon/glass carriers. For the time being, this limit is still unclear.



Source: IBM

[Use of an organic multilayer interposer for BGA packaging use](#)

Who should be interested in this report?

Integrated semiconductor Device Manufacturers and fabless semiconductor companies

- Visualize the drivers and expected benefits by application of 3D silicon/glass interposers as well as the alternative options
- Benchmark the industrialization status of 3D glass/silicon
- Identify possible partnership /or second source packaging subcontractors for your forthcoming developments

Assembly and Test Service companies

- Get the list of the main companies involved in 3D silicon/glass interposers development and industrialization
- Screen possible new applications and technologies to support diversification strategy with 3D silicon/glass interposers

Silicon Wafer foundries

- Screen possible new applications and technologies to support diversification strategy with 3D silicon/glass interposers, especially by loading aging facilities

Equipment and Material suppliers

- Understand the differentiated value of your products and technologies in this emerging but fast growing market
- Identify new business opportunities and prospects

Electronic module makers and Original Equipment Makers

- Evaluate the availability and benefits of using 3D silicon/glass interposers in your end system
- Monitor different 3D silicon/glass interposers suppliers to adjust your sourcing strategy

PCB and IC substrate manufacturers

- Monitor the evolution of IC packaging, assembly and test, especially linked to the emerging 3D silicon/glass interposers
- Measure the threat of 3D silicon/glass interposers to the established PCB interposer and substrate businesses
- Screen possible new applications and technologies to support diversification strategy with 3D silicon/glass interposers

Companies cited throughout the report

AAC Microtec, Allvia, AMD, Altera, Amkor Technology, apm, ASE, ASET, Avago Technologies, Bridgelux, CEA-LETI, ChipMOS, Cree, Corning, Dai Nippon Printing, Dalsa, Discera, Elpida, Epcos, Epistar, EPWorks, Fraunhofer IZM, Georgia Tech, Hitachi, Hymite, Hynix, Ibiden, IBM, IME, IMT, Infineon Technologies, Intel, Ipdia, Liquid Design Solutions, LG Innotek, Lumileds, Maxim, Micron, Nanium, National semiconductor, NEC / Schott, Nepes, Nichia, Nippon Electric Glass, Nokia, NXP Semiconductors, On Semiconductors, Panasonic, Qualcomm, Renesas, Replisaurus Technologies, Samsung, Schott, Sensoror, Shinko Electric, Silex Microsystems, SMIC, Soitec, Sony, StatsChipPac, STEricsson, STMicroelectronics, Süss Microtec, Tecnisco, Texas Instruments, TMT, Toshiba, TSMC, UltraTech, UMC, UTAC, VTI Technologies, WLCSP, Xilinx, Xintec

Historical account

From 2D to 3D silicon/glass interposers



2.5 IC Enables Device Function Partitioning for Cost Performance

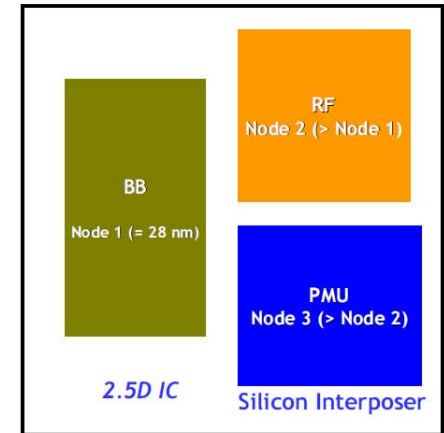
- Some companies promote 2.5D interposers so as to optimize the use of the various technology nodes at their maximum integration potentials according to the functions to be designed, for example:

- Digital on CMOS 28nm
- RF on CMOS 90nm
- PMU on CMOS 130nm

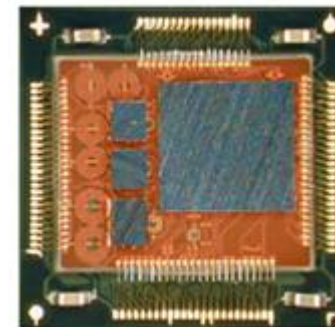
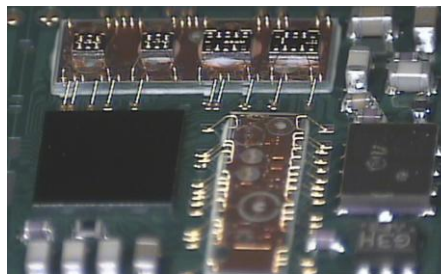
- However, since many SoC's are already packaged by flip-chip, the opportunity to turn back to wire bonds is questionable, and true 3D silicon/glass interposers may well be needed in the near future for high IO count / high IO toggling frequency devices.



28 nm
(Single-chip
Package)

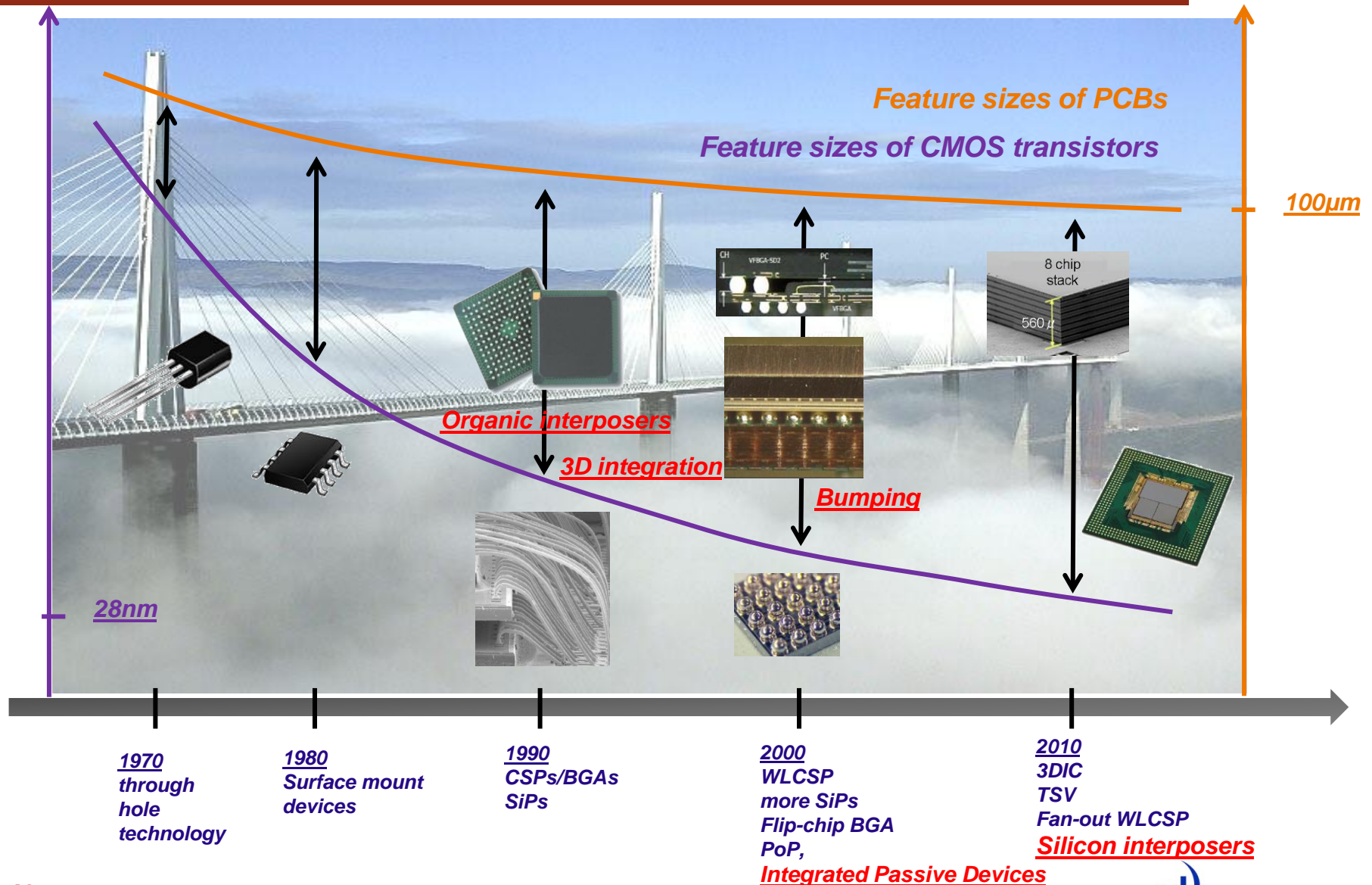


Courtesy of ASE



Courtesy of STMicroelectronics

The evolution of semiconductor packaging: a bridging technology between ICs and PCBs



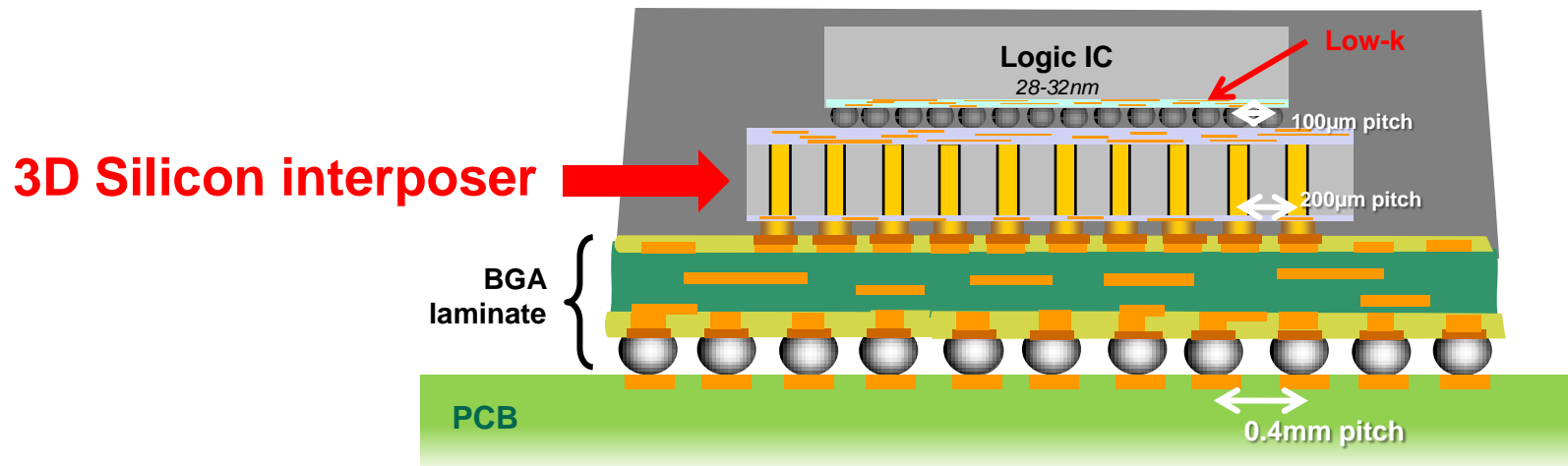
The evolution of substrate technologies

- In the next 5 years, packaging substrates are expected to integrate significantly higher pin counts and embedded active and passive devices within System in Package (SiP) configurations.
- Minimum line width will shrink to 5 microns with less than 30 microns to 5 microns via diameters:
 - To fabricate such ultra higher density packaging substrate, current PWB process technology will face to technology limitation → Possibility to introduce **silicon interposer** and/or **glass interposer** like LCD panel to fabricate less than 5 microns wiring with much smaller via diameters.

	2000 – 2005	2006 – 2010
Technology Driver (Min. Line Width)	30µm – 15µm Flip Chip	15µm - 5µm - 3µm Flip Chip, EAD/EPD for SiP
Via Diameter	75µm – 50µm	30µm – 5µm
Capital Investment	\$0.15 – \$0.20 Billion	US\$ 0.20 – 0.50 Billion
Major Process	Semi Additive	Semi Additive. Silicon Technology & LCD Technology (Glass Substrates)
Bus Frequency	8000 MHz – 1.2 GHz	> 10 GHz
Package Type	CSP, WL-CSP	PoP, CSP, BGA/CSP with Embedded Active & Passive Devices
PWB Type	Builup PWB, FPC, FRPC	Silicon &/or Glass Interposer , Buid-up PWB
Application driver	Cellular phone, Digital Home Appliances, Broad-band Internet	Digital TV, Smart Phones, Digital Home Appliance
Profit Structure	High Added Value & Differentiate	High Added Value & Differentiate
Business Model	Core Competence + Horizontal Division of Labor	Core Competencies + Strategic Alliance + New Concept

More Silicon Value is Moving to the Package!

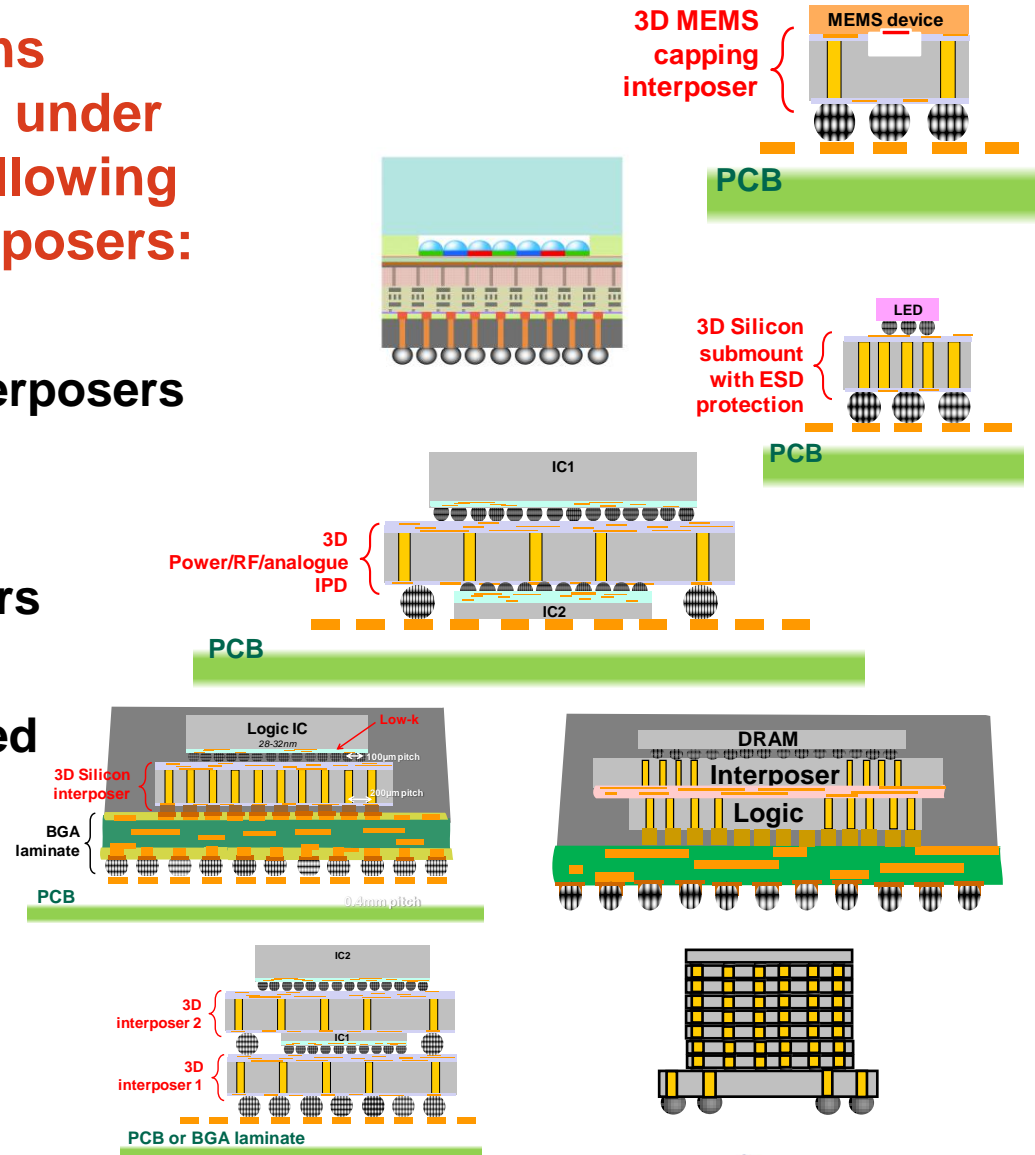
- **A recent trend increasing these days are 3D interposers:**
 - Based on silicon or glass, 3D interposers are a next generation substrate technology which aims at replacing traditional PCB laminate or ceramic technologies for the sake of extreme miniaturization and performance. This type of “intermediate 3D” is perceived as a **“bridge” platform** between today’s 2D and future genuine 3D that will start beyond 2012-2013. Specific features like the integration of mature logic and analog functions such as IPD (integrated passive devices) will be key components in the effective commercialization of 3D interposers in the short term.
- **3D integration opens up a possible supply chain value change to all players:**
 - As more and more value is now moving to the package in general. IDMs, Fab-less players, wafer Foundries, packaging houses, MEMS players, substrate and PCB suppliers are all poised to take on more value in this new era if they all prepare for the investments it requires!



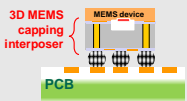
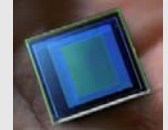
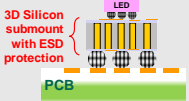
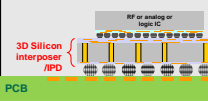

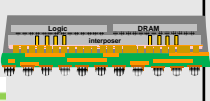
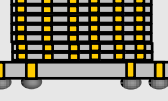
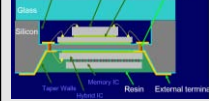








Silicon/glass 3D interposers technology segments

- By studying exhaustively solutions currently in production as well as under development, we identified the following technology segments for 3D interposers:

- MEMS and sensors capping interposers
- Logic only interposers
- Logic + memory interposers
- CMOS image sensors interposers
- HB-LED silicon submounts
- 3D Power/RF/analogue integrated passive interposers
- Memory stack interposers
- Miscellaneous silicon/glass substrates/packages



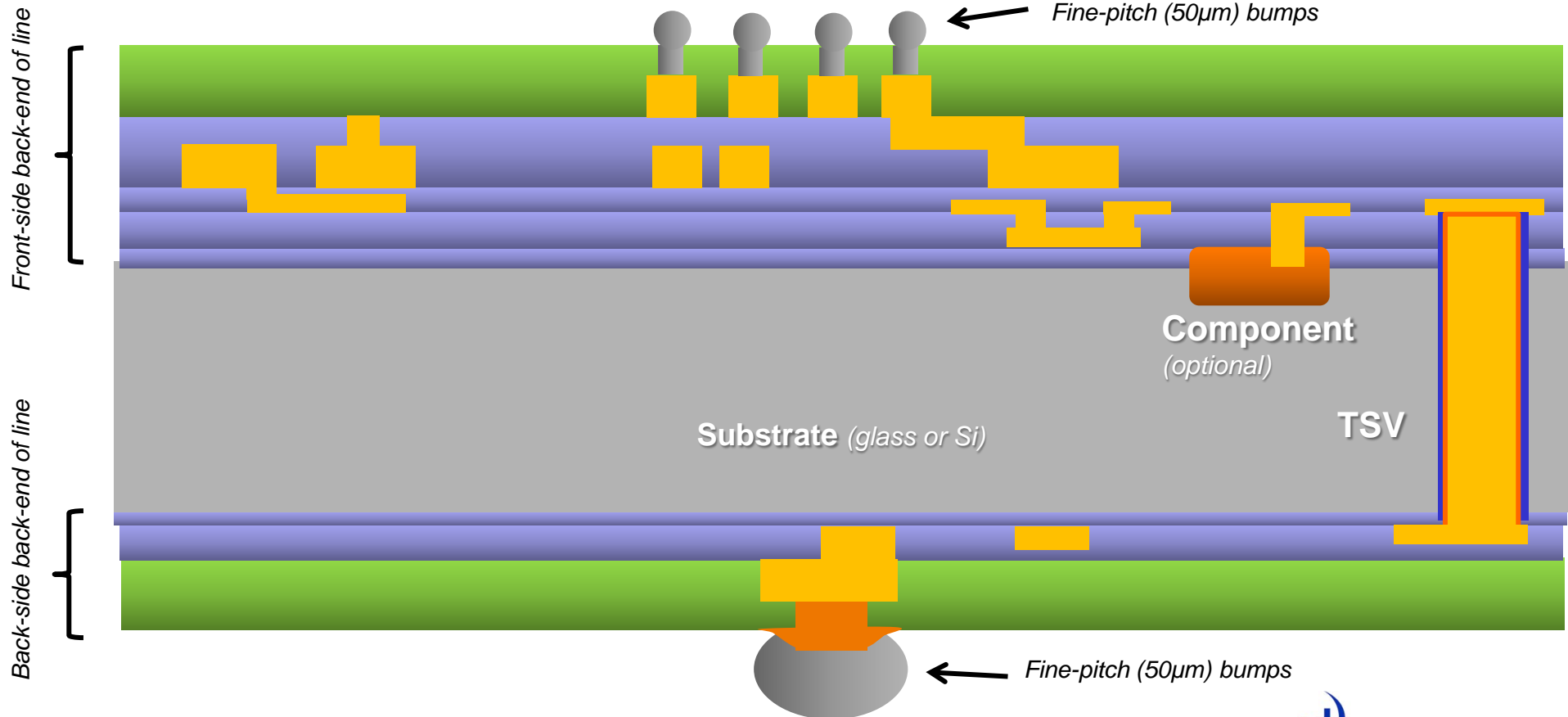
Summary table - 2010 Status of 3D silicon/glass interposers an emerging market

								
Interposer type (technology segments)	MEMS and sensors capping interposers	CMOS image sensors interposers	HB-LED silicon submounts	3D Power/RF/ analogue integrated passive interposers	Logic only interposers	Logic + memory interposers	Memory stack interposers	Misc. Silicon/glass substrates/packages
Applications	gyroscopes, accelerometers, microphones, pressure sensors, RF-MEMS, microfluidic, micro-probes, optical	CIS (in mobile phones, cameras, automotive)	HB-LED/ UHB-LED (mobile, automotive, general lighting)	RF transceivers and power amplifiers (mobile phones, medical & industrial)	High IO count logic IC's: CPU's, GPU's, FPGA's, application processors	Application processors for mobile phones, CPU's, GPU's	Server farms, computers, both DRAM's and flash memories	Medical, industrial, oil search, aerospace, defence
2010 status	In Production	Sampling. Will appear with BSI. Sony already in BSI, w/o interposers	Some early production	Sampling (similar interposers, but w/o TSVs are in production)	Proofs of concepts	In-development, proofs of concept	In-development, start of prod by year end	Development of demonstrators
Wafer size	150-200mm	300mm	150-200mm	150-200mm	300mm	300mm	200mm	150-200mm
2010 Wafers	183k (86-inch) 44k (8-inch)	0	50k (6-inch eq.)	A few hundreds	0	0	A few k's	A few hundreds
Players (non-exhaustive)								

3D silicon/glass typical interposer structure & definitions

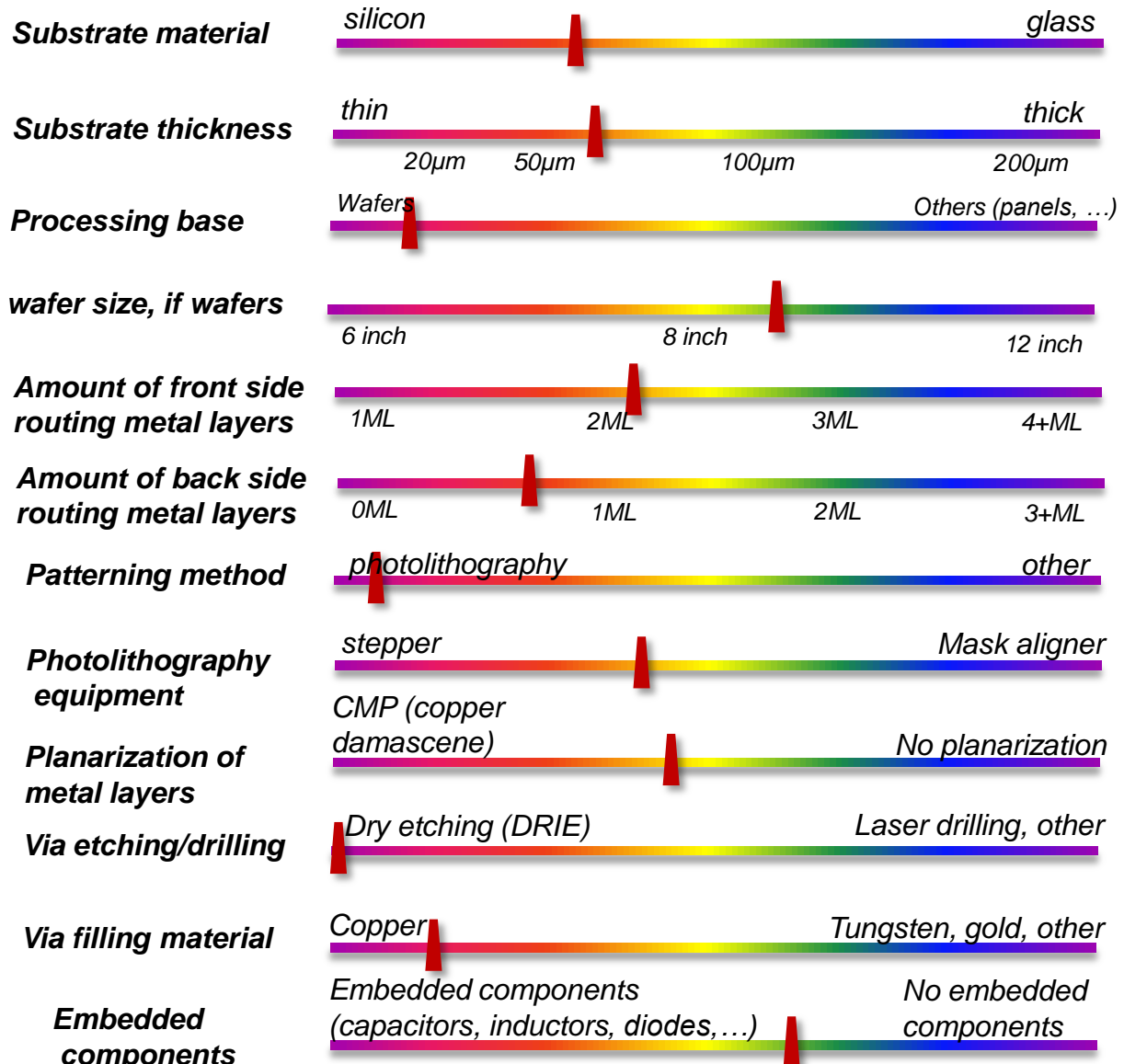
Generic Cross-section drawing

-  **UBM** (*under Bump Metallurgy*)
-  **Metal** (*Al or AlSiCu or Cu or W*)
-  **ILD** (*Inter Layer Dielectric, SiO2 or Si3N4 or polymer...*)
-  **Dielectric passivation** (*Polyimide, BCB, epoxy, AL-X*)



3D silicon/glass interposer technology options

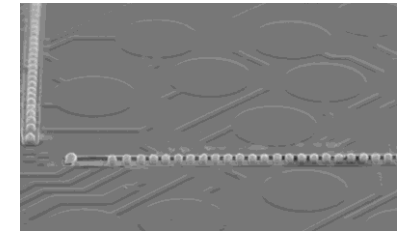
The average interposer is rather ...



Substrate



Back-end of line



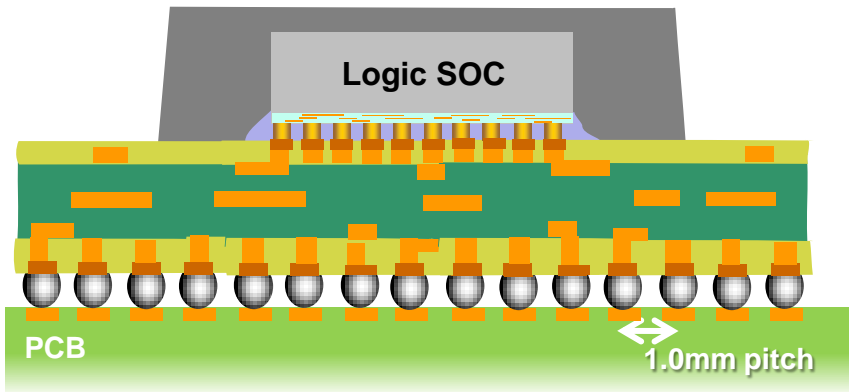
Vias



3D Silicon interposer Case example #1:

220µm pitch Flip-chip down to 1.0mm PCB (3/4)

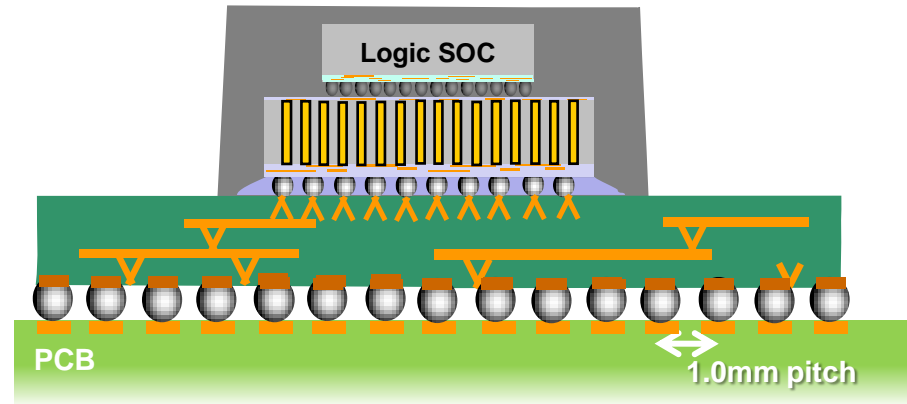
FC-BGA solution (1+2+1)
for 220µm pitch Flip-chip to 1.0mm PCB



TOT Packaging COST = \$2.40

3D interposer solution

Interposer (Glass or Silicon)
+ cheap BGA (2 layers) solution

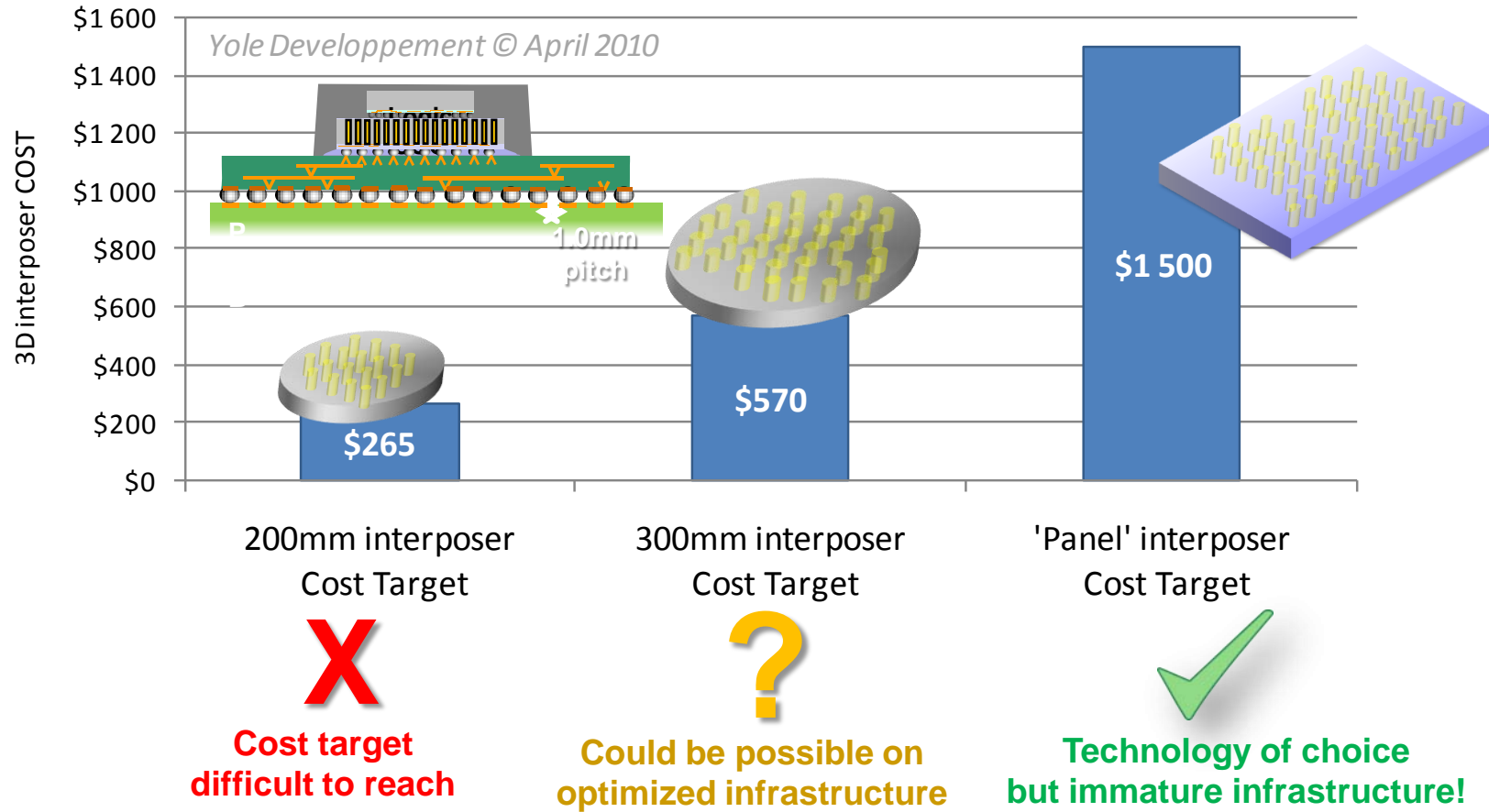


TOT Packaging COST = **\$1.9 - \$2.1 !**

3D Silicon interposer * Case example #1:

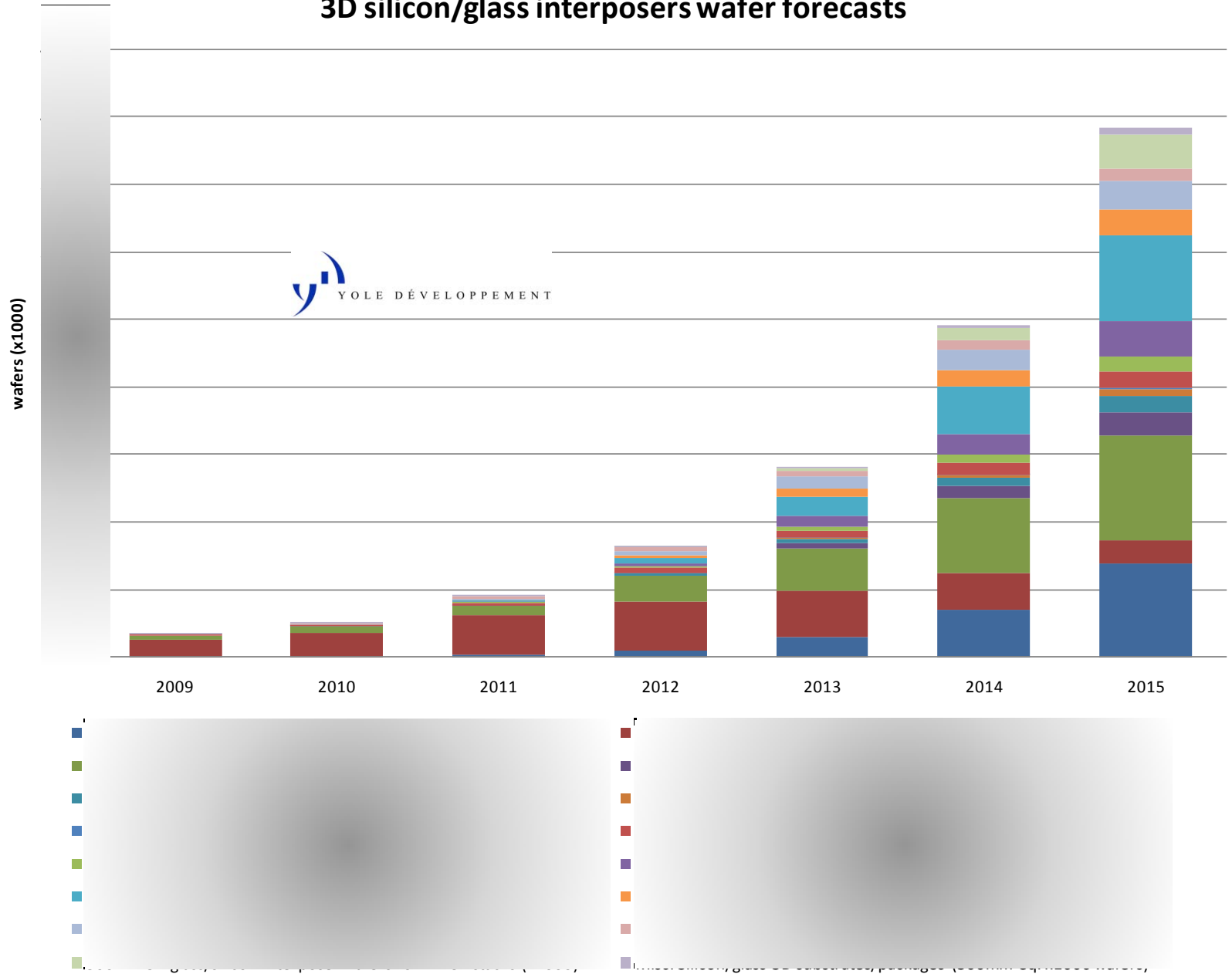
3D interposer COST target to reach parity with FC-BGA equivalent solution (for Application #1)

* 3D Interposer cost include metal vias + RDL



Silicon Interposers market forecasts

3D silicon/glass interposers wafer forecasts



About the Authors of this Report

- **Jean-Marc Yannou:**

- Jean-Marc is in charge of advanced packaging analyses at Yole Développement, including Wafer Level Packaging and 3D System Integration. He has 15-years of experience in the semiconductor industry. He worked for Texas Instruments and Philips (then NXP semiconductors) where he served as “Innovation Manager” for System-in-Package technologies



- **Jerome Baron:**

- Jerome is leading the MEMS and Advanced Packaging market research at Yole. He has been involved in the technology analysis of the 3D packaging market evolution at device, equipment and material supplier levels. He was granted a Master of Science degree in Nanotechnologies from the National Institute of Applied Sciences in Lyon, France

