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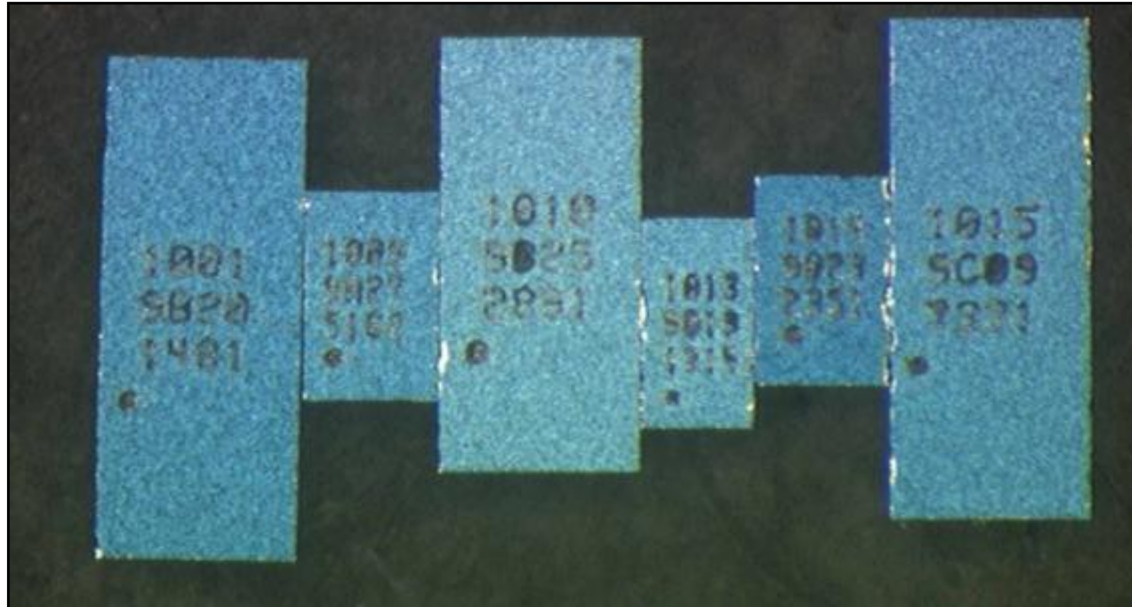
Reverse Costing analysis



Efficient Power Conversion GaN transistors
(EPC 1001 – 1009 – 1010 – 1013 – 1014 - 1015)

July 2010 - Version 1

Written by: Sylvain Hallereau

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Product Identification

The devices subject to teardown for this work are six EPC enhancement mode gallium nitride on silicon power transistors. Six devices are analyzed. The devices are sold as solder-bumped bare dice.

Devices analyzed

EPC device	V rating	Rmax (mOhm)	Die size (mmxmm)	Markings line 2	Markings line 3
1015	40	4	4.1x1.6	9C09	7333
1014	40	16	1.7x1.1	9?23	2353
1013	150	100	1.7x0.9	9D13	1321
1010	200	27	3.6x1.6	9B25	2893
1009	60	30	1.7x1.1	9B22	5164
1001	100	7	4.1x1.6	9B20	1481

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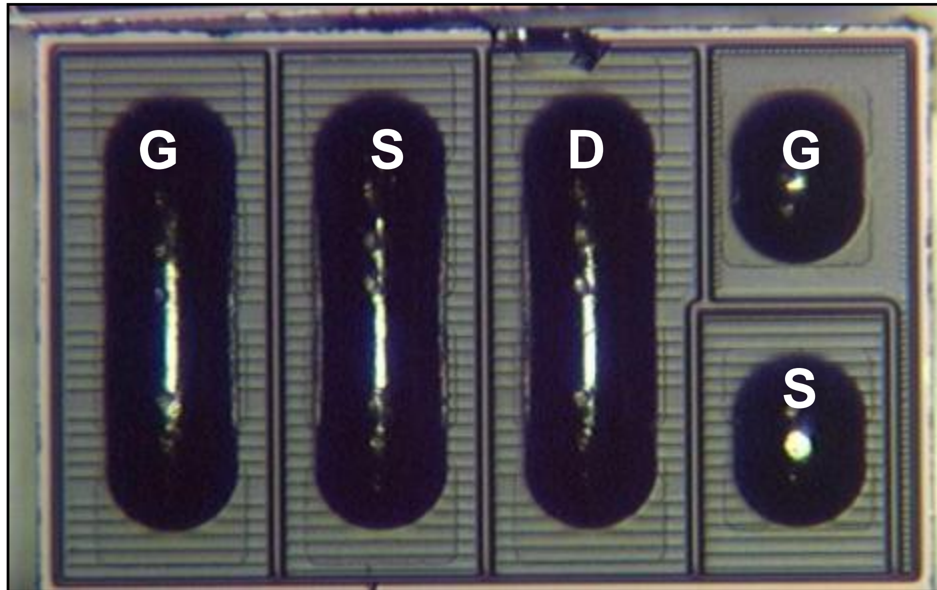
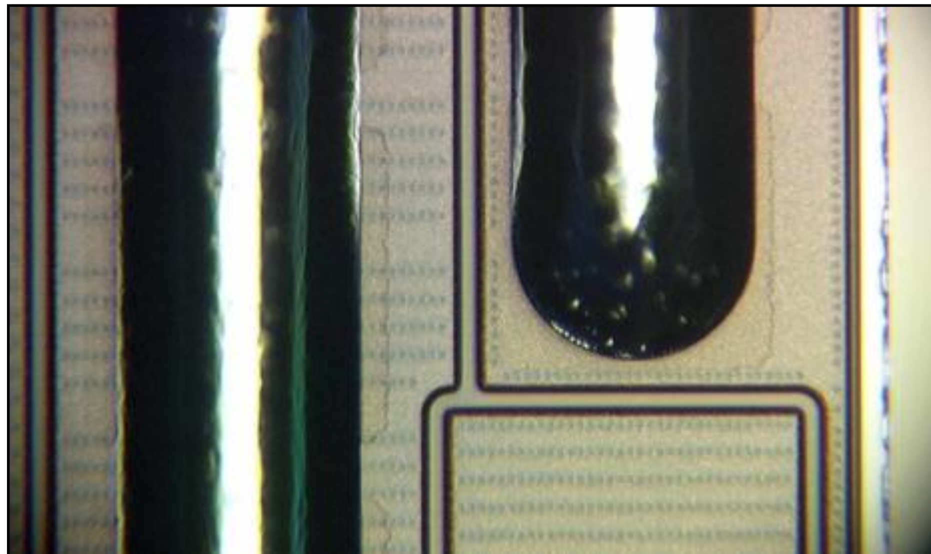
Plan view analysis



Device 1009.

All devices are built in the same way. Longer devices have more alternating S-D solder bumps.



There are three layers of metals, plus the solder bumps.

Each solder bump lies on a Metal 3 plate, connecting to Metal 2 by rows of contacts.

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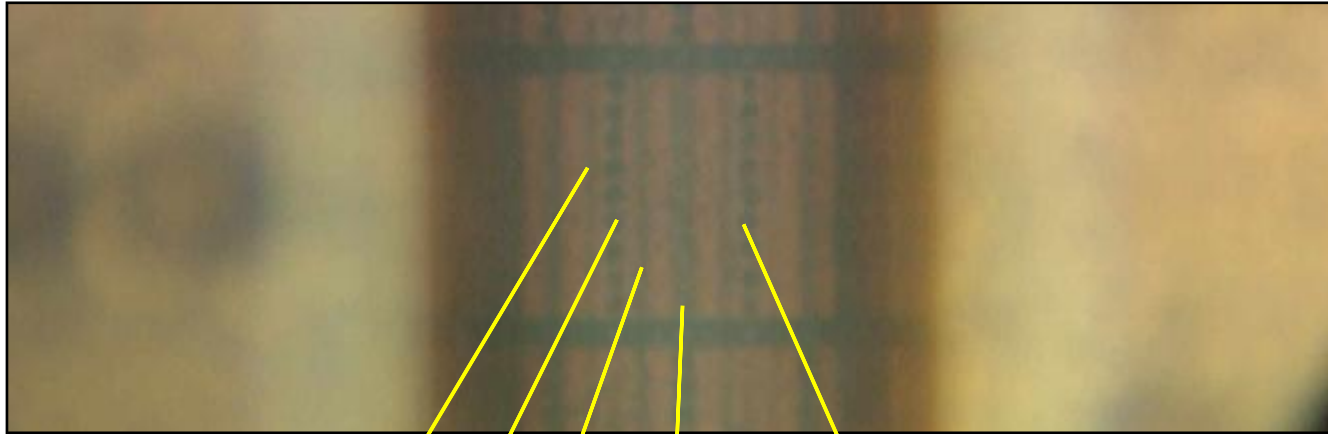
Gate – Source - Drain



M3

M2

M1

source

drain

gates

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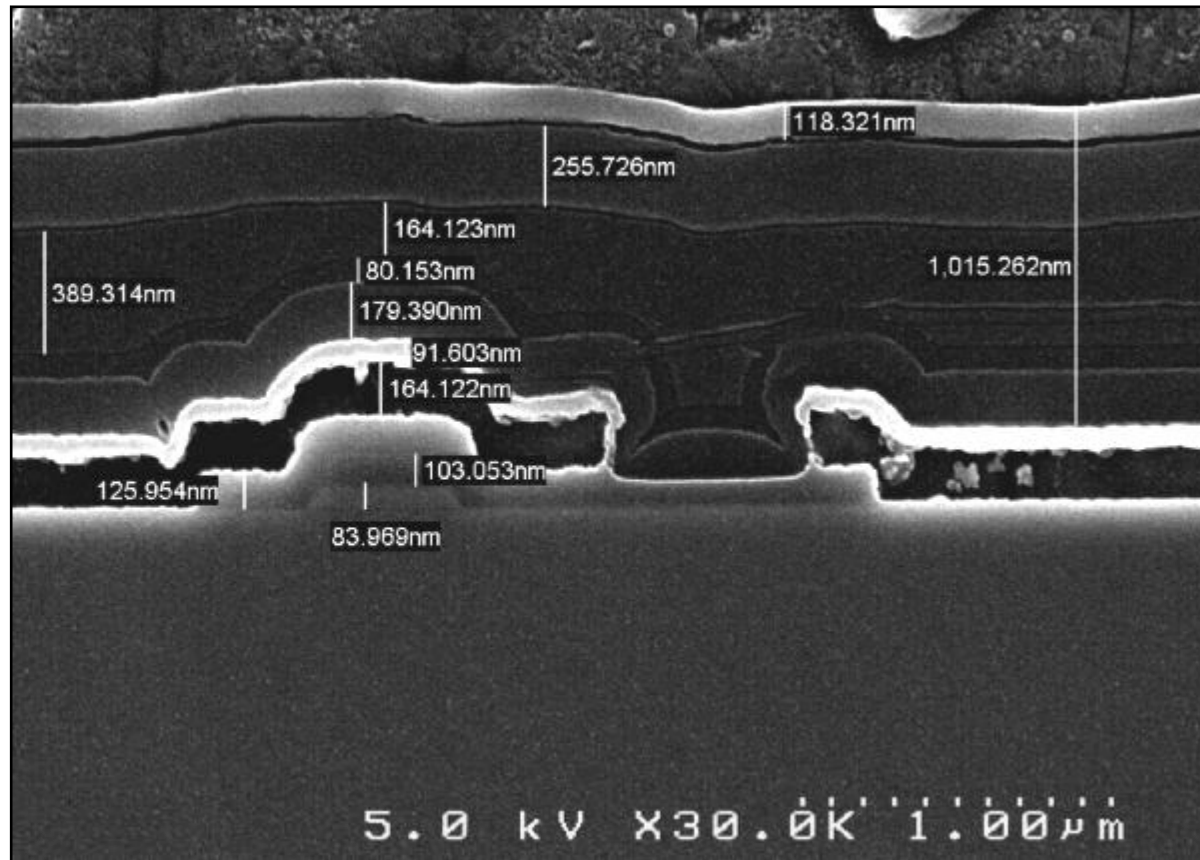
Intermetal Dielectric



Details of the intermetal dielectric between Metal 1 and Metal 2. After the patterning of M1, a highly conformal oxide is deposited, creating re-entrant corners. Layers of what appears to be spin-on-glass are used to restore planarity before the vias are opened for the tungsten plugs and the subsequent deposition and patterning of the die-length Metal 2 strips.

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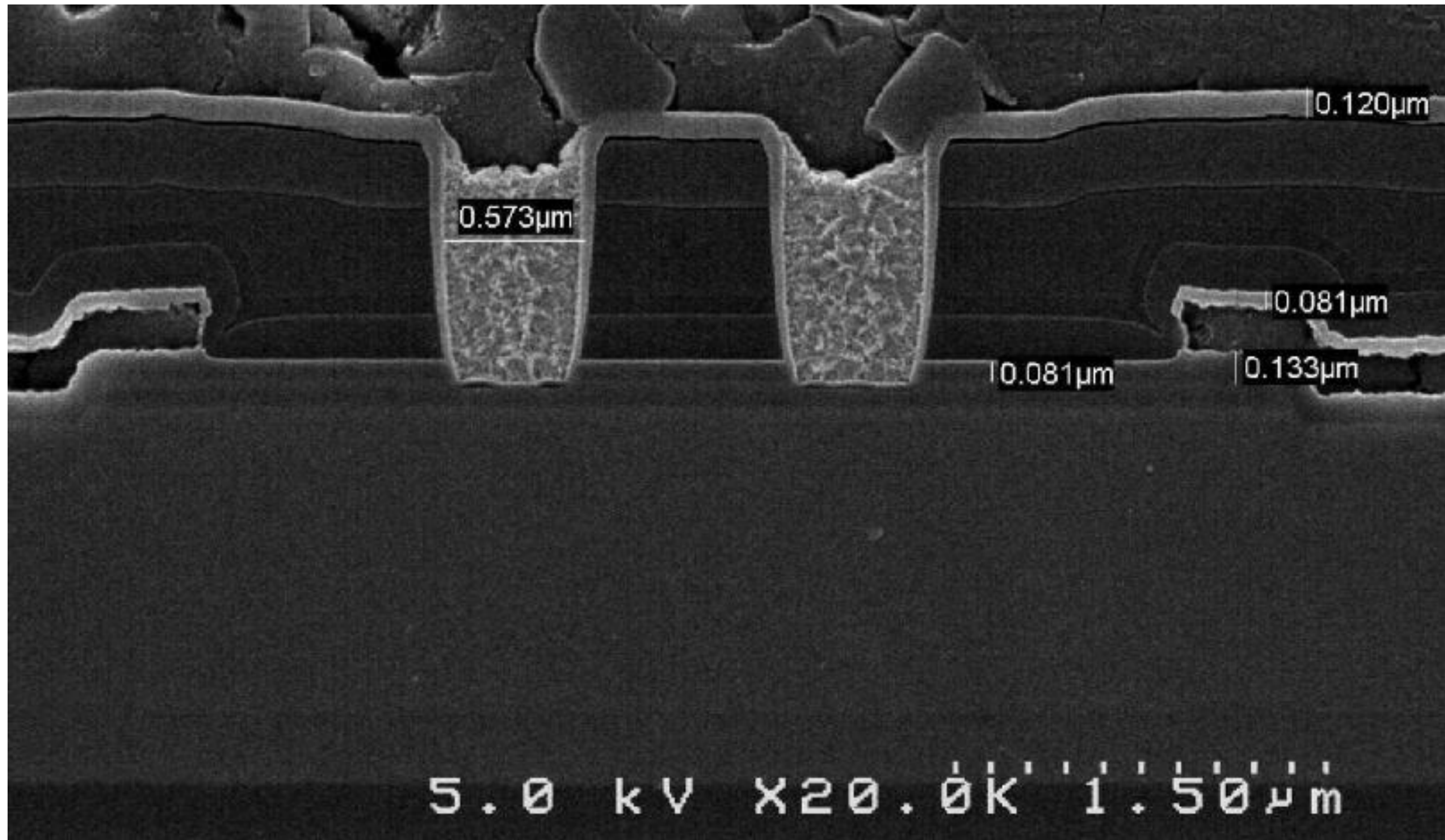
W Plugs



The W plugs are 0.5um in diameter.

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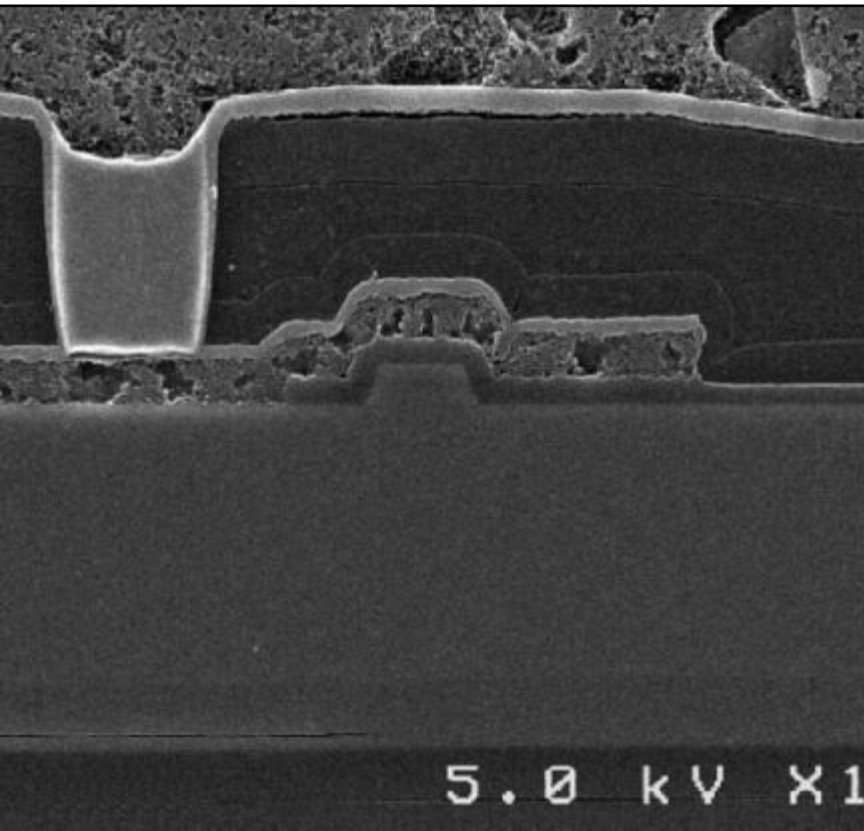
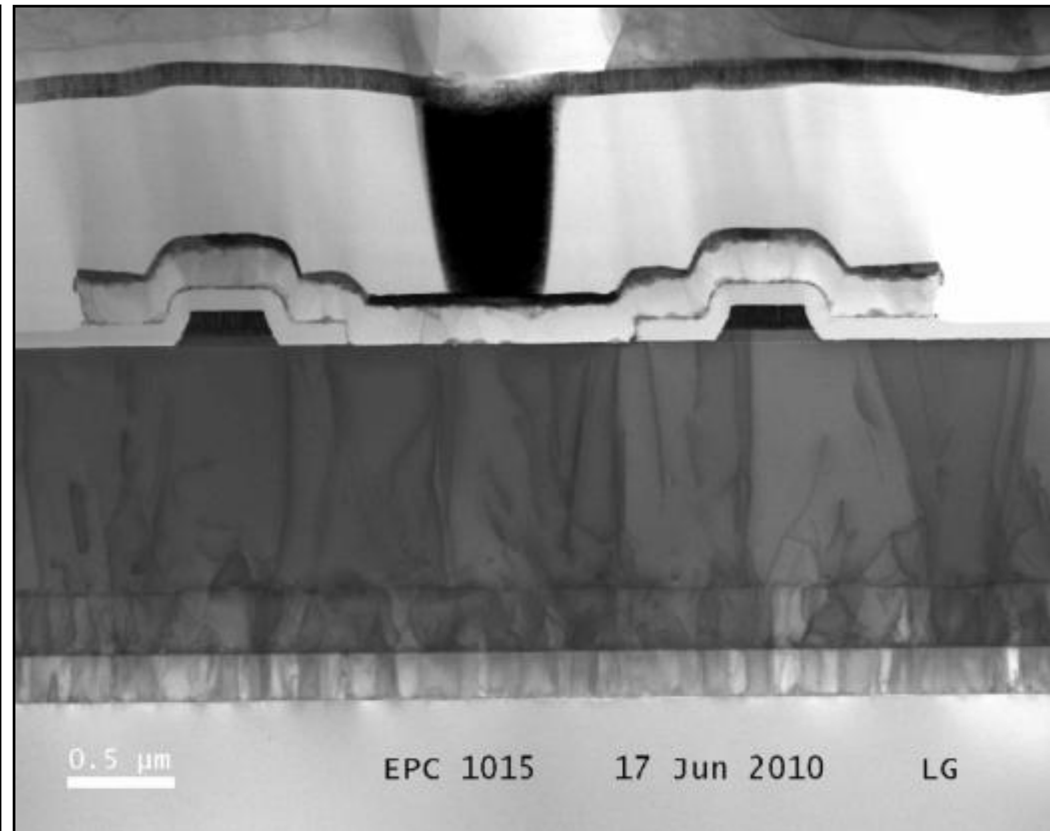
Front End Process





Higher magnification SEM (left) and TEM (right) cross-section view of transistors and the GaN layers

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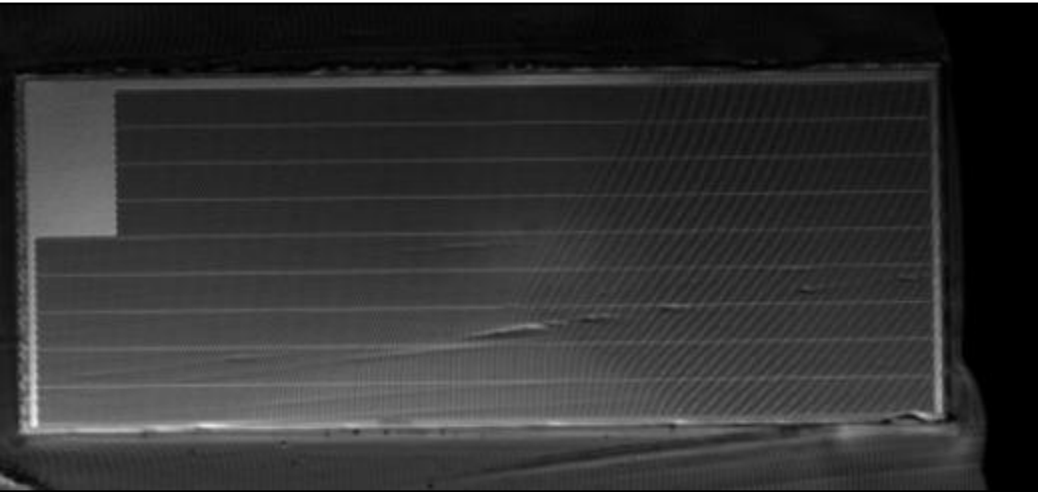
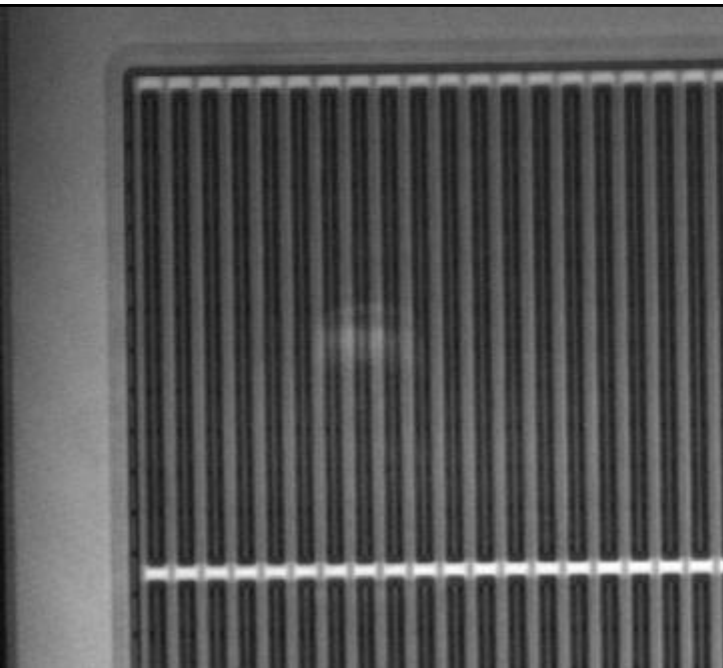
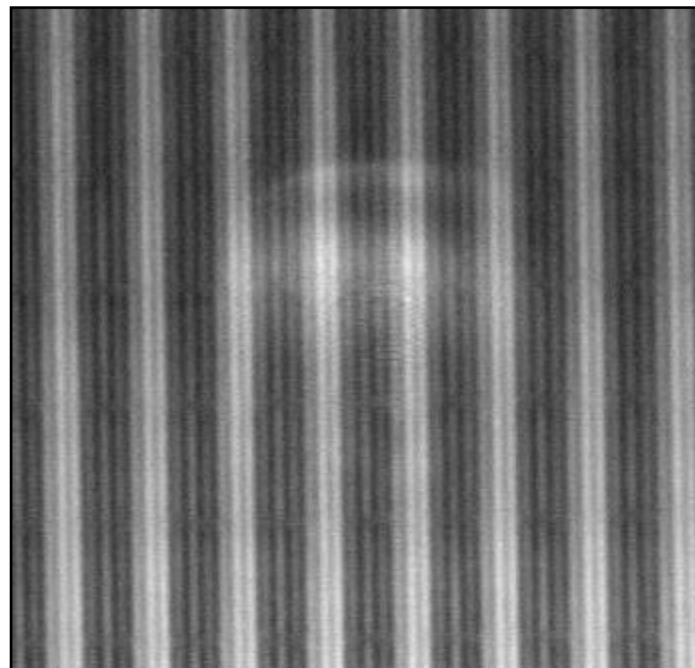
Device dimensions - 1001



General overview of device 1001. The white rectangle is the gate contact pad. The horizontal white lines are gate contacts.





Images with the 50x objective. Zoom 1 (left) and zoom 3 (right). The thin white lines are the source contact; the fatter gray lines are the drain contacts. Individual gates are not resolved.

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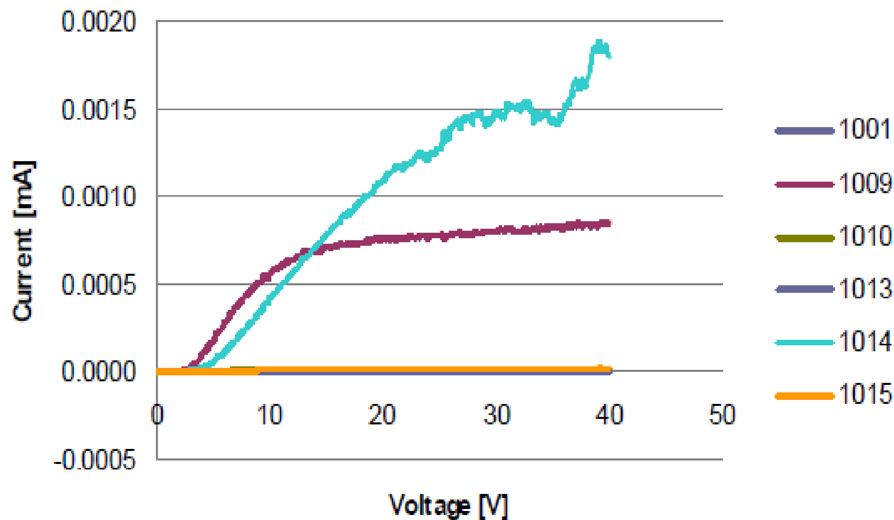
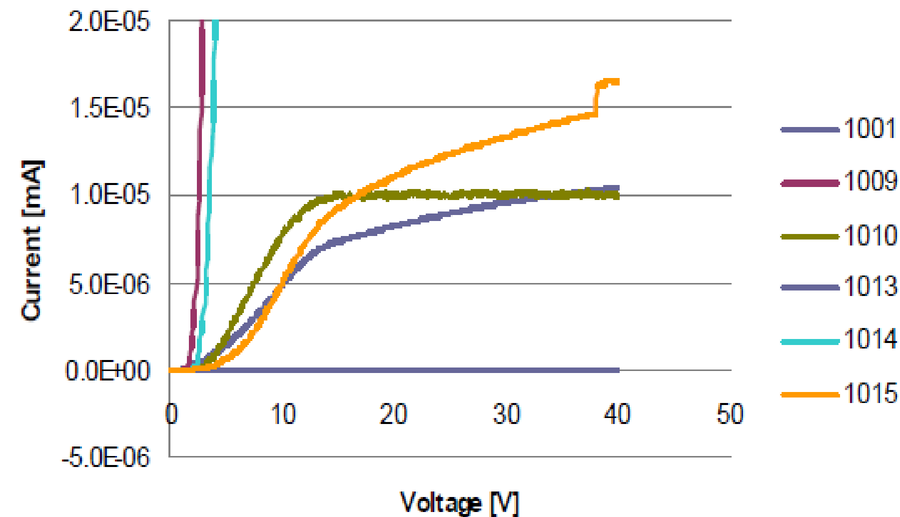
IDss

For this measurement the Gate is tied to the Source (VGS=0) and VD swept from 0V to 40V measuring Drain current. Both graphs show the same data but with different vertical scales.





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Transistor Process Flow

Transistor

[illegible]

The main parts of the process:

Transistor

(1) [illegible]

(2) [illegible]

(3) [illegible]

(4) [illegible]

Metal Layers

(1) [illegible]

(2) [illegible]

(3) [illegible]

(4) [illegible]

(5) [illegible]

(6) [illegible]

Metal Layers

[illegible]

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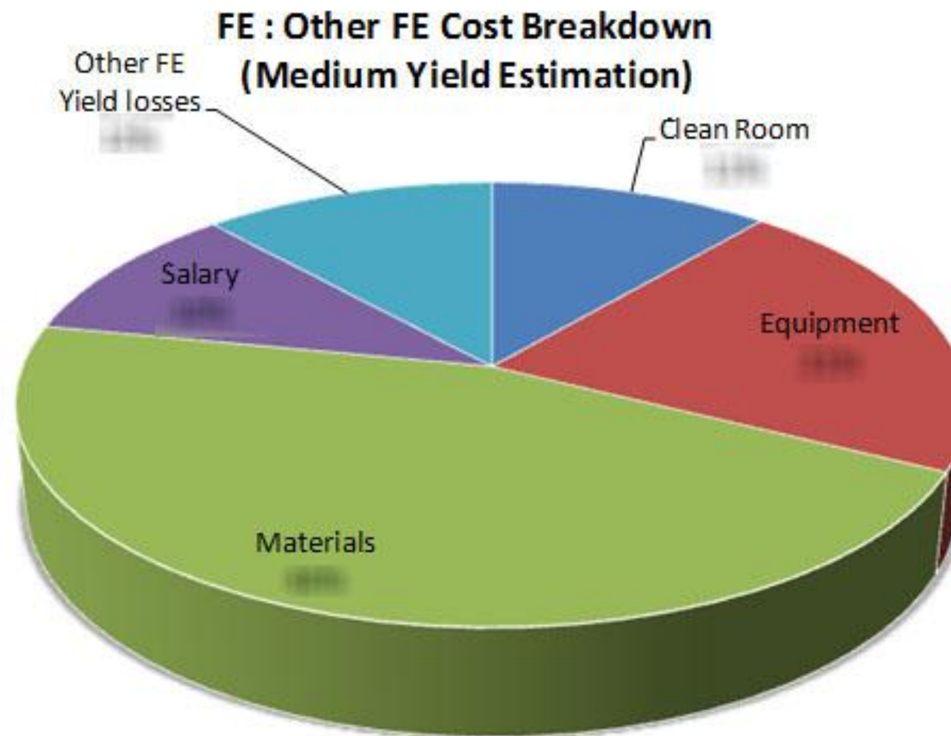
GaN transistor Total Front-End Cost

Total Front-End	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Raw Substrate Cost (Si)	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
FE : Epitaxy Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
FE : Other FE Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
FE : Yield Losses Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
TOTAL Front-End Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]



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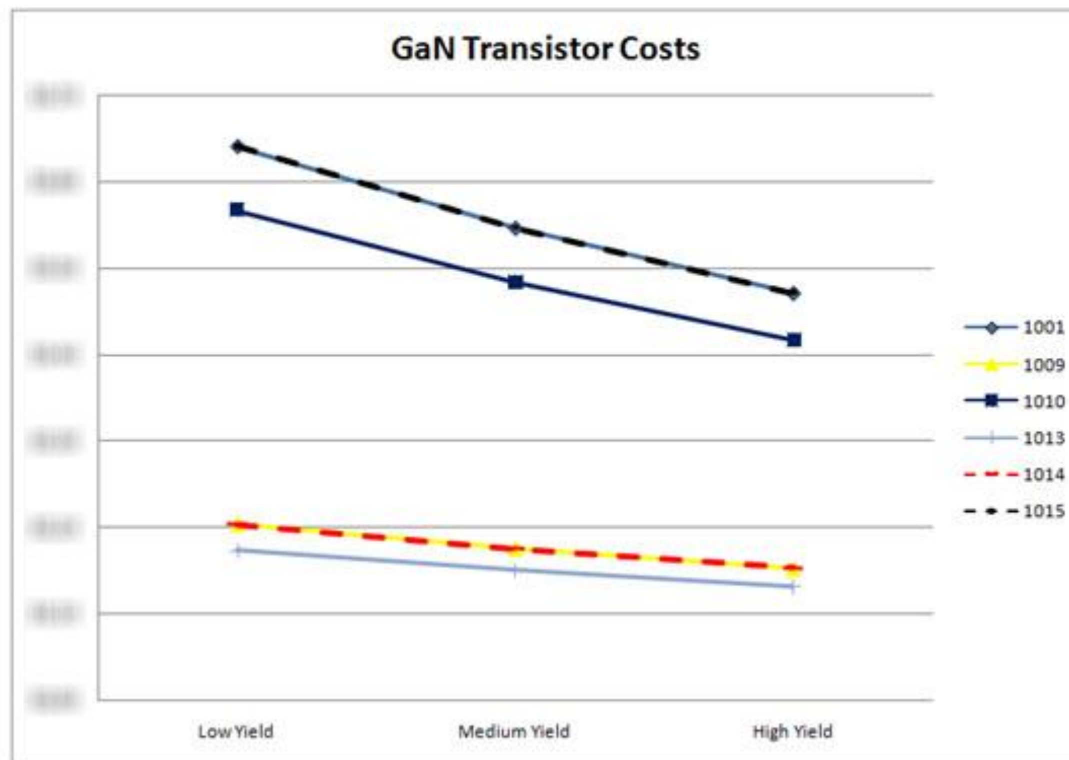
Component Manufacturing Cost

Die Cost	1001	1009	1010	1013	1014	1015
V rating	100V	60V	200V	150V	40V	40V
Id	25A	6A	12A	3A	10A	33A
Die Area (in mm²)	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Low Yield	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Medium Yield	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
High Yield	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]



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