LED Packaging 2011

A comprehensive survey of the main LED packaging technologies and market metrics.

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Scope of the Report (2): Process Steps

This report covers the Back-en level 0 and level 1 of the High Brightness LED manufacturing process

Substrate

SiC
Sapphire
Silicon
Bulk GaN
Composite substrates

Front end Level 0: Epitaxy
- Nucleation layer
- n type layer
- Active layers (MQW)
- p-type layer

LED epi-wafer

Front-End Level 1: Device Making
- Inspection
- Masking / Lithography
- Etching
- Metallization/contacts/mirrors

Mesa LED structure
Flip Chip LED structure
Vertical LED structure

LED dies-on-wafer

Back-End (Packaging) level 0:
- Laser Lift-Off (LLO) – Substrate separation - Bonding
- Die singulation
- Testing and Binning.

LED dies

Back-End (Packaging) level 1:
- Die Attach and interconnect
- Phosphor
- Encapsulation and optics
- Testing and binning

Packaged LED

Sources: Yole Développement

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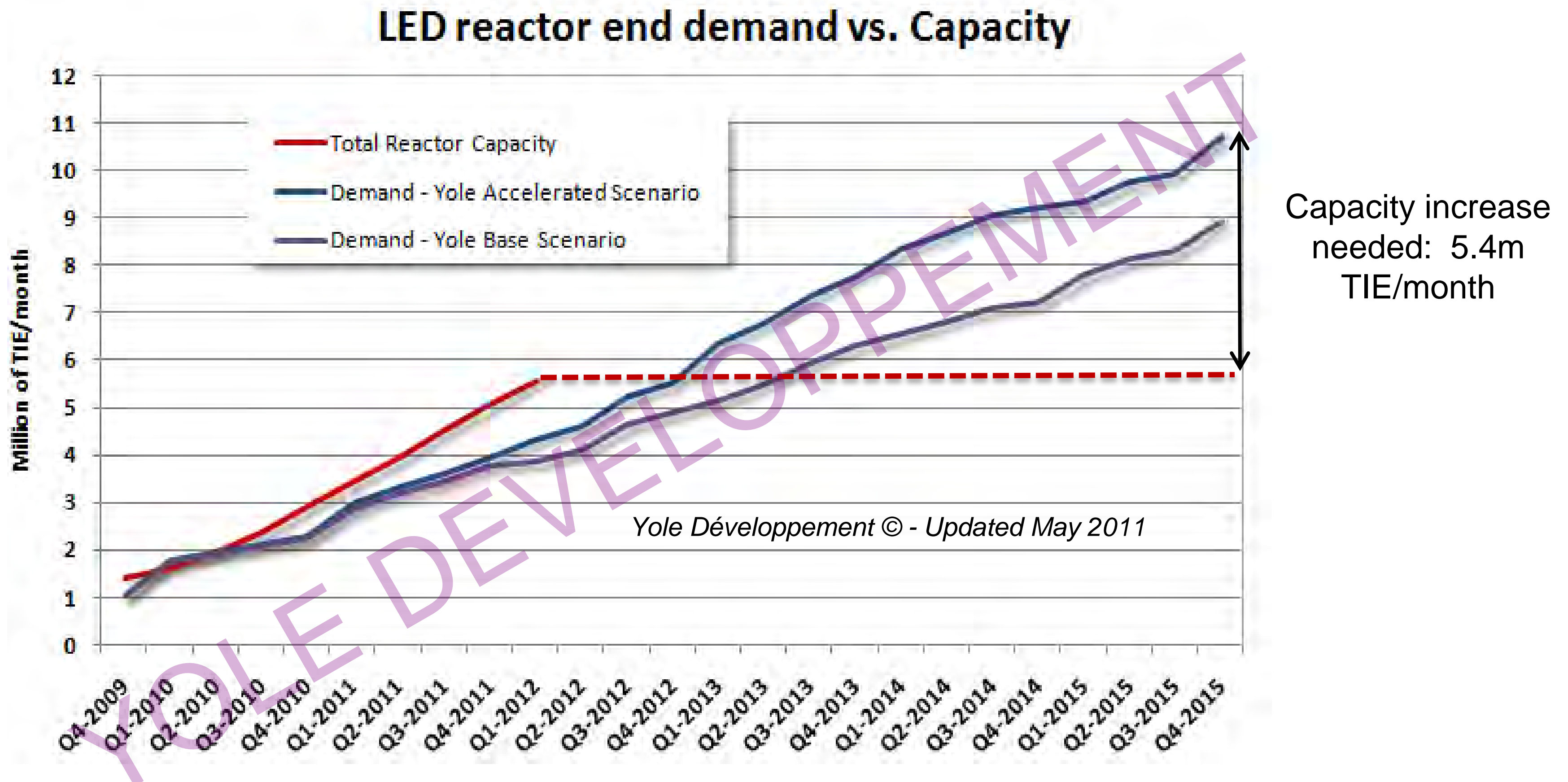
GaN Capacity vs. Demand:



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- MOCVD reactors shipment volume is a good metric to gage the overall equipment market.
- After the tight supply situation experienced in early 2010 for packaged LEDs, the current equipment investment cycle driven by massive investments in China will lead to an overcapacity buildup that could take 12-24 months to absorb.
- However, our accelerated scenario calls for a minimum 5.4 million of Two Inch Equivalent (TIE) per month reactor additional capacity necessary for the 2012-2015 period. Considering a typical average industry utilization rate of 85%, this number could realistically be up to 7.2m TIE.

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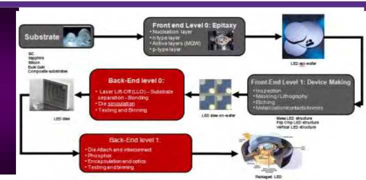
Typical Process Flow:



EpiWafer Bonding
Carrier wafer
Epiwafer

Substrate Removal
Carrier wafer
Epitaxial substrate

Wafer Inspection / Defect Mapping

Wafer Probing
(Electrical / Optical)

Wafer Backgrinding Die Singulation

Die Inspection,Testing & Sorting

Die Attach
Die
Package Substrate

Interconnect

Phosphor & Encapsulant

Lens attach or molding
Lens

Testing and Sorting

Osram Oslon

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- Exact process is product dependant and varies from one manufacturer to another. For example substrate removal and wafer bonding are only used for the manufacturing of vertical LED structures, But some manufacturers of vertical LEDs use technologies that don't require wafer bonding. Numbers and positions of testing and inspection steps can also vary.

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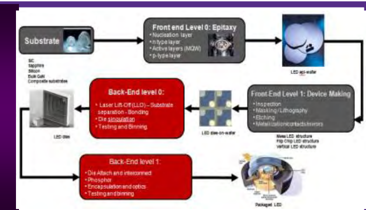
GaN LED Chip Design Overview:
Trends:



Structure	Trends	Comment
p- electrode; Contact layer*; p- GaN layer; Active layers; n-GaN layer; Mirror Layer; Contact layer; n- electrode; Sapphire substrate — Standard MESA Structure	→ (flat)	- Standard mesa structures remain the most cost effective solution for applications and design requiring low current densities (→ low heat generation)
n-GaN layer; Active layers; p- electrode; Sapphire substrate; p-GaN; n- electrode; Solder Bump; Metal; Metal — Flip Chip MESA Structure	↗ (rising)	- Flip chip designs have been widely adopted by Philips Lumileds for all their GaN high power packages that are being increasingly used for general lighting and automotive applications. Other manufacturers are using Flip chip designs on a case per case basis.
p- electrode; Contact layer; p- GaN layer; Active layers; n-GaN layer; Metal Substrate — Vertical Structure with substrate removal	↗ (strongly rising)	- Vertical LED structures are being increasingly adopted for a wide gamut of high power applications. Pioneered by Osram and Semileds, the design has now been adopted in many products by Cree, Lumileds, LG and others.
p- electrode; Contact layer; p- GaN layer; Active layers; n-GaN layer; Conductive Substrate — Vertical Structure on conductive epitaxial substrate (SiC, Si, ZnO..)	↘ (declining)	- The only commercial products based on an electrically conductive substrates are CREE chips that are grown on SiC. However, CREE is increasingly adopting vertical LED design where the SiC epitaxial substrate is removed and replaced by a carrier substrate or submount (Silicon)

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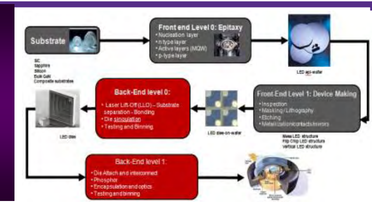
High Power LED Packaging
Overview



Die Attach → Interconnect → Substrate (Thermal Management) → Phosphor (White LED only) → Encapsulation

- **Die Attach / Interconnect:**
  - Eutectic Bonding
  - Stud bump (Flip chip)
  - Epoxy / Conductive Epoxy
- **Interconnect:**
  - Ball/Wedge wire bond
  - Ribbon Bonding
  - Via through Die and/or Submount / Ceramic
- **Substrate:**
  - Substrate Only: *Ceramic, Metal, Silicon*
  - Substrate (Ceramic, Metal, Silicon) + Si Submount
- **Phosphor:**
  - Dispersion
  - Conformal coating
  - Ceramic
  - Remote Phosphor
- **Encapsulation:**
  - Encapsulation + 1 or 2 lenses – Silicon or Epoxy

Wafer Level Packaging

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High-Power LEDs include one or multiple chips. A very large gamut of packaging technologies is being used for High Power LEDs in order to handle the higher power density and manage the large amount of heat generated by the dice. There are no standard. Each design is unique in its form factor, die and packaging technology, choice of substrate materials, and the way those technology bricks are combined.

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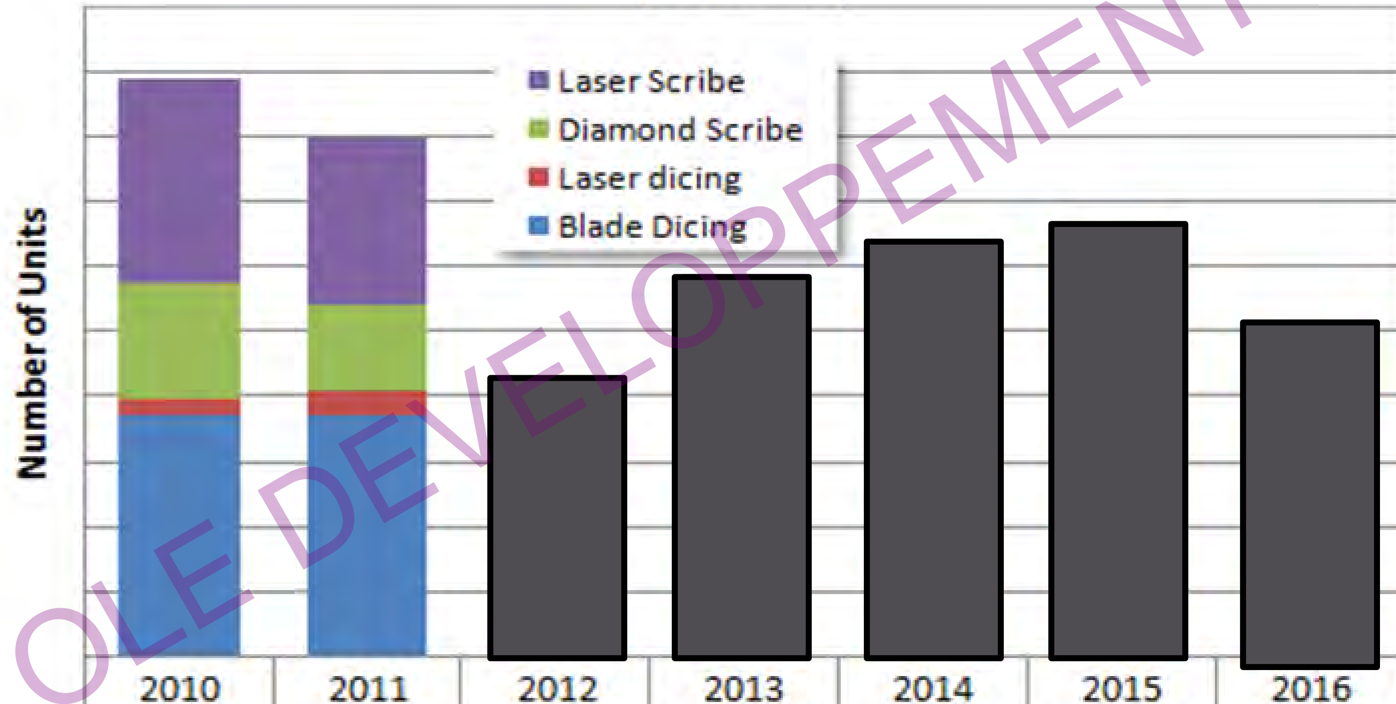
Singulation Equipment Market: Volumes

Singulation Equipment For HB LED Annual Sale
(Volumes)



	2010	2011	2012	2013	2014	2015	2016
Laser Scribe	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Diamond Scribe	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Laser dicing	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Blade Dicing	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

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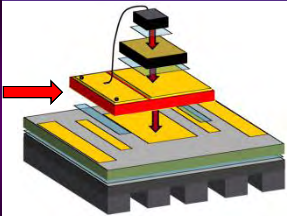
Substrates for mid-power LEDs
Trends



- Technologies are well established and relatively standardized for low and mid power LEDs. However, large LCD backlight are driving some changes in the mid power category:
  - Adoption of “Multichip” packages with 2 chips.
  - Increase of the average power and light output, taking the chips used for this application closer to high power chips in term of thermal management solutions:

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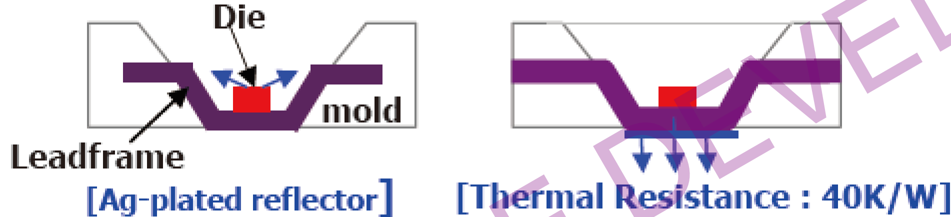
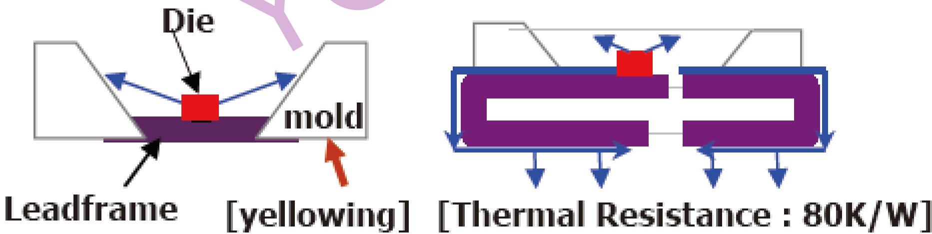
SLED Leadframe structure for Heat dissipation(1)



Conventional L/F structures



Example of evolution of lead frame structure for mid power chips used in TV backlight applications (source: Samsung LED)

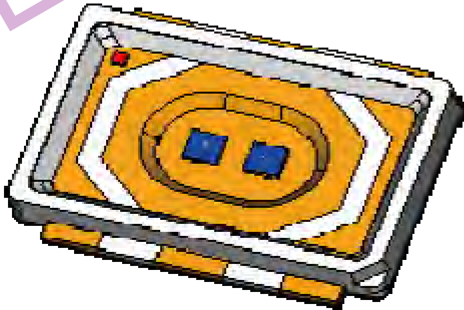
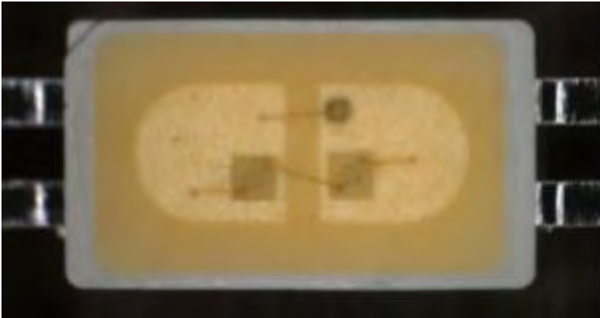


Illustration of 2 die mid power chips (source: Samsung LED)



Picture of 2 die mid power chips (source: Assymtek)

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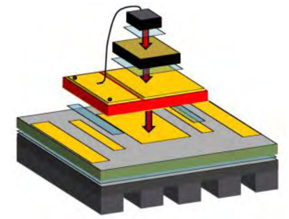
High Power LED Substrate
Market Penetration Forecast by substrate type



High Power LED substrate market shares
by substrate type

Legend
COB (MCPCB or Ceramic)
SMT Glass-Ceramic
SMT 3D Silicon
SMT Metal leadframe
SMT Ceramic DPC AlN
SMT Ceramic DPC Al2O3
SMT Ceramic LTCC Al2O3/AlN

Y-axis: 0%, 10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, 100%

X-axis: 2010, 2011, 2012, 2013, 2014, 2015, 2016

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Note: technology adoption rates for <u>High Power</u> (>1W) LED package <u>only</u>

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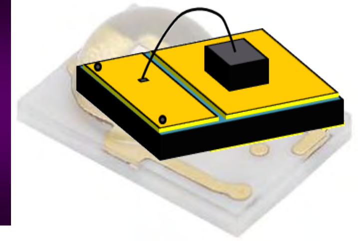
Interconnections:

Flip Chip Layout Principles and Technologies illustration: Lumileds Luxeon Rebel (1)



Contact to upper (p-GaN) level

Contact to lower (n-GaN) level

Bump

(a)

(b)

Redistribution Layer

Contact to Lower Active Layer

Contact to Ohmic Metal

Die Bump Location

Approximate location of gap in package metallization

(c)

Gold

Aluminum

Dielectric

Adhesion Layer

Silver

Tungsten

Titanium

Gallium Nitride

p-n Junction Region

Schematic diagram of LED device structure. Note that this is inverted from the SEM images, as the die is flip chip.

(d)

Bump

Top layer contact

Lower layer contact

Pictures and drawings are by courtesy of System Plus Consulting

(a) x-ray picture of substrate metal layers through LED die and bumps

(b) Drawing of LED front (bottom) side layout

(c) Drawing of LED cross-section with contacts

(d) Picture of LED die front side

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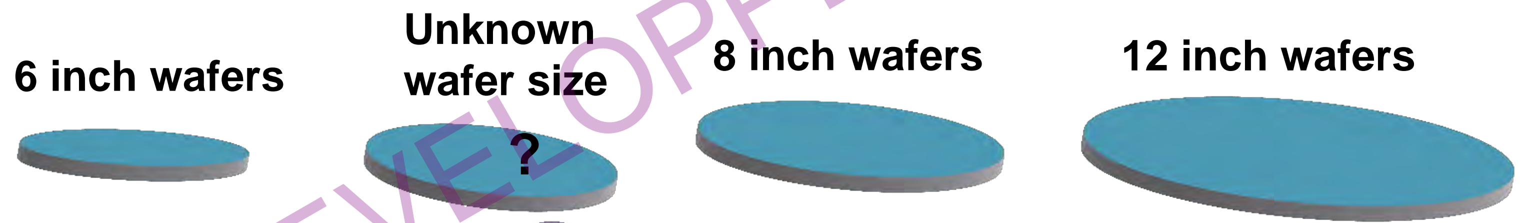
Silicon Substrate and WLP for high power LEDs
Main actors by wafer sizes (R&D or production)

- Only a handful of players are currently working on silicon substrates, either on 6 or on 8 inch wafers.
- We expect silicon substrates to gain momentum as more operations are done at the wafer level, and on larger wafers. Thisway, silicon substrates will enable low cost assembly of high power LEDs.



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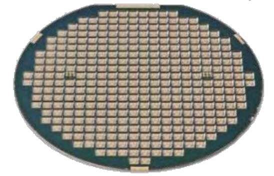
Silicon Substrates and WLP
Example: VisEra technology (TW)

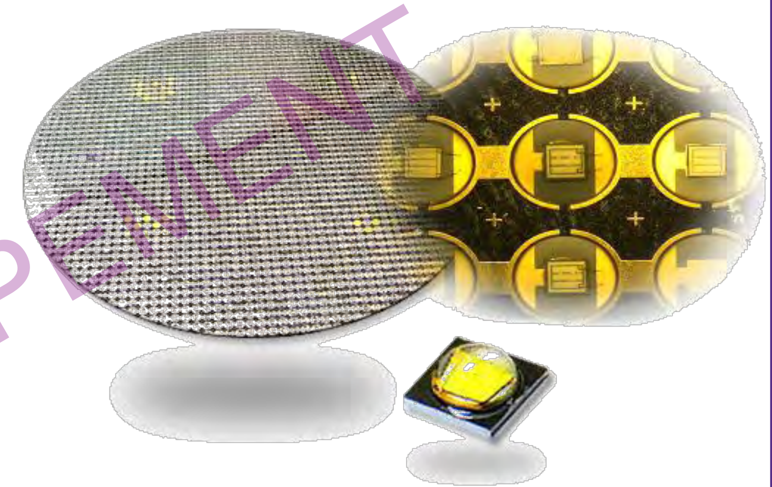


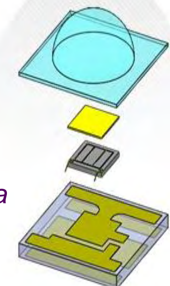
- **TSMC and subsidiaries VisEra technologies and Xintec technologies announced a High-Power LED packaging technology based on XX inch wafers**

- **Technology blends MEMS process and proprietary TSV techniques with wafer-level phosphor conformal coating and lens molding.**

- **Main Features:**
  - **Mass production (low cost)**
    Current capacity > XX M units/month
  - **Low thermal resistance (as low as 2°C/W)**
  - **CTE compatible**

- **Currently available as a foundry service, TSMC might leverage on the platform to speed up its entrance into the LED industry.**





Courtesy of VisEra

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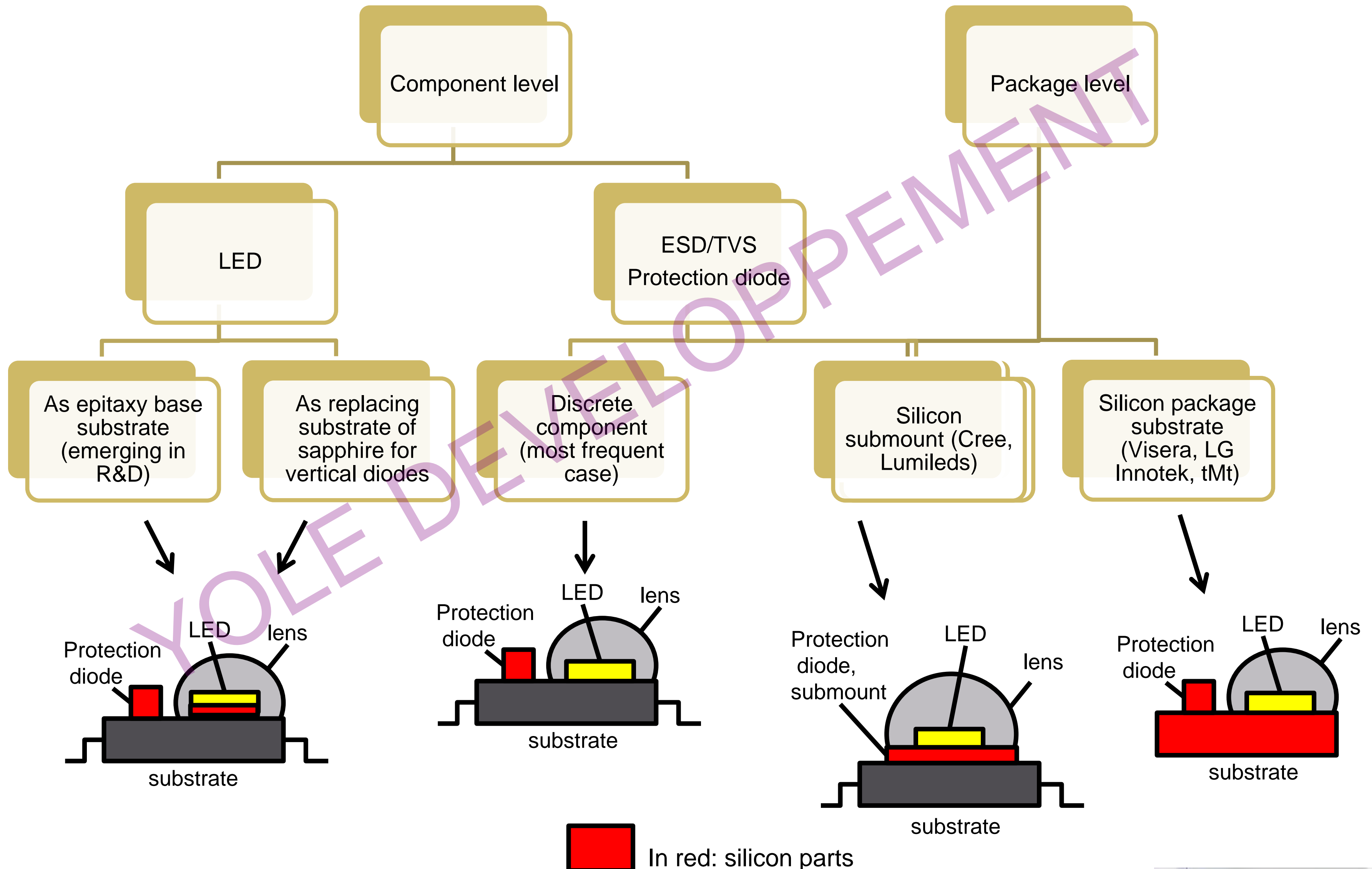
Silicon in high power LED Packages
various uses



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