



*Thin Si Wafer on Carrier (Courtesy of EVGroup)*

## 3DICs bring opportunities, challenges

There certainly isn't a 'one-size-fits-all' approach to 3DICs, but it's a huge business opportunity with the potential to dramatically shake things up in the semiconductor industry.

Only a few years ago, the semiconductor industry was still debating whether or not 3DICs would ever really take off. But the industry quickly accepted 3D as a viable path forward—aggressively pursuing it, finding ways to remove the hurdles, work with the technology, and actually implement it.

Moving forward, many key decisions must be made and, as always, there will be more challenges to maneuver around. Confusion still surrounds the emerging 'mid-end' area in wafer processing, and the lack of standardization is also a concern for many. This time around, the changes aren't just in technology: We're already starting to see signs that equipment makers will be affected by consolidation.

And since materials will play a pivotal role in the future of 3DICs and other wafer-level packages, it's a good time to also take a look at what's going on there and see where they're headed.

### Emerging 'mid-end'

With a convergence of front-end and back-end companies pursuing opportunities in the confusing zone of overlap in wafer-level packaging between the back-end-of-line (BEOL) and back-end packaging, the term 'mid-end' is now being used to describe it. This includes not only 3DICs with TSVs, but also fan-in wafer-level packages, fan-out wafer-level packages (FOWLP), flip chips, and embedded die.

Not everyone is happy with the usage of this term, however, because they still see distinctly different companies with different business models and believe that front-end equipment manufacturers' move into the back-end has less to do with 3D technology and more to do with a lack of opportunities in the front-end.

Regardless, the term 'mid-end' is likely to stick and gain traction to describe this zone of overlap, as many companies are seeing this convergence.

"We're seeing a convergence in the 'mid-end' of the semiconductor industry on multiple levels," explains **Thorsten Matthias**, director of business development at EV Group. "Processes and technologies, which used to be purely front-end, back-end, or assembly, are now being moved across all areas. For example, in the past, oxide wafer bonding was primarily used for silicon-on-insulator (SOI) wafer manufacturing, so basically pre-front-end. Now it's used for backside-illuminated image sensors. And it becomes even more difficult to distinguish between front-end, back-end, and assembly when you create a stacked system such as MEMS-on-ASIC-on-logic. Also in the mid-end area, we have a convergence of industries such as VLSI-ICs, power electronics, compound semiconductors (CS), and MEMS. Vertical interconnects and vias have been used in CS and MEMS for many years."

In terms of TSVs, both IDMs and OSATs are pursuing various 'mid-end' types of structures. "We consider these mid-end types of structures to be TSVs between 100 to 200µm deep, with aspect ratios from 5 to 15," says **Arthur Keigler**, chief technology officer and vice president of advanced technology at NEXX Systems. "Most of these are in the range of 100 to 120µm deep, with an aspect ratio between 8 to 10. Lower aspect ratio TSV is being used now in development mode to take advantage of existing tool sets by some customers, but we see movement to higher aspect ratios as process and tool sets become more affordable."

In plating, there are also signs of convergence, bridging IDM/foundry and OSAT, according to **Steve Lerner**, CEO of Alchimer SA. "Unfortunately, we're not seeing it to the extent that it should be happening," he notes. "Litho requirements are very different for each of the specified user segments. PCBs and LCDs tend to be panel-driven, while IDM/foundry and OSATs are solidly wafer-driven. Dry tools typically used in the front-end are trying to make their way into the OSAT arena, but we feel that approach is holding back progress because the OSATs won't be able to afford such infrastructure."

The main drivers of the 'mid-end' in 2010 were flip chip and wafer-level chip-scale packaging (WLCSP), and it looks like fan-out wafer-level packaging (FOWLP) may see significant growth in 2011, followed by 3D TSV technologies in 2013 and beyond.

### Front-end companies reaching into the back-end

We've started to see many traditionally 'front-end' equipment companies start pursuing opportunities in what has been considered, until very recently, 'back-end' territory.

For successful entrance into any market, clear differentiation must be established, points out **Damo Srinivas**, senior director of business development for Novellus' equipment portfolio serving the advanced wafer-level packaging applications.

"Novellus has introduced several significant technology advancements to aid in overcoming challenges associated with TSV integration, including robust, repeatable TSV fill, minimization of overburden and wafer bow, and mitigation of the thermomechanical stability issues inherent in a copper/silicon system," Srinivas elaborates. "Cost, of course, has been a major hindrance to TSV integration, and minimizing process time as well as reducing the cost of consumables are areas Novellus has innovated. Clearly, with any new market penetration, platform manufacturability and reliability are key questions, and our strategy across our suite of 3D products has been to heavily leverage our production-proven productivity-leading front-end platforms and technologies, while optimizing the specific package for back-end integration cost and technology needs."

It's worth noting that there's a significant difference in how work is performed in the front-end vs. back-end. The back-end has a much greater cost sensitivity and cost pressures. "You're forced to take the cost out of processes very aggressively in the back-end, while in the front-end it's more about ensuring processes work and guaranteeing the processes and supporting customers with any issues they may have," notes **Wilfried Bair**, SUSS MicroTec's vice president of strategic business development.

The 3DIC market shows the greatest potential for significant future growth in the semiconductor industry. It's a huge business opportunity, as Bair explains. "How often does a business opportunity to do something fundamentally different come along in this industry? The 3D technology is fundamentally changing how processing is done and offers the

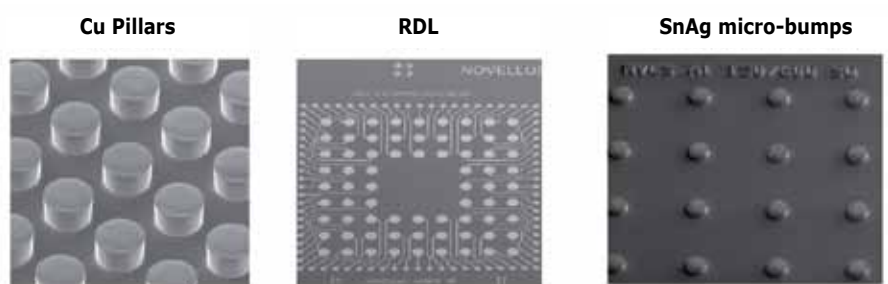
opportunity for new equipment modifications," he says. "Large equipment makers like Applied or TEL and others in that category or size typically aren't interested in anything with \$100-150M equipment revenue, but the 3D market promises at least several hundred million for each new product type—so it's of great interest."

### Materials development for 3DICs and other wafer-level packages

Materials will continue to play a pivotal role in the evolution of 3DICs and other wafer-level packages. The good news for materials is, as **Phil Garrou**, an industry consultant through his company Microelectronic Consultants of NC, and also a senior analyst for Yole, puts it: The process options have narrowed considerably since 2008, so basically now we're looking at 'via-middle' processes coming from the fabs and 'backside via-last' most likely coming from the OSATs, when just two years ago there were more than 10 process sequences all in contention.

Along with technical challenges ahead, there are many other nontechnical, market-driven issues that need to be addressed, according to JSR Micro's **Mark Davis**, product manager for packaging materials, and **Jim Chung**, program manager in emerging technologies. They point out that unlike FEOL processes, for which consortia or alliances pull resources together to solve technical challenges and set process development directions, the 'mid-end' market is much more fragmented and lacks the needed infrastructure. The result is smaller, individual companies tackling technical problems independently rather than working together using common platforms, and the result is unintentional perpetuation of market fragmentation.

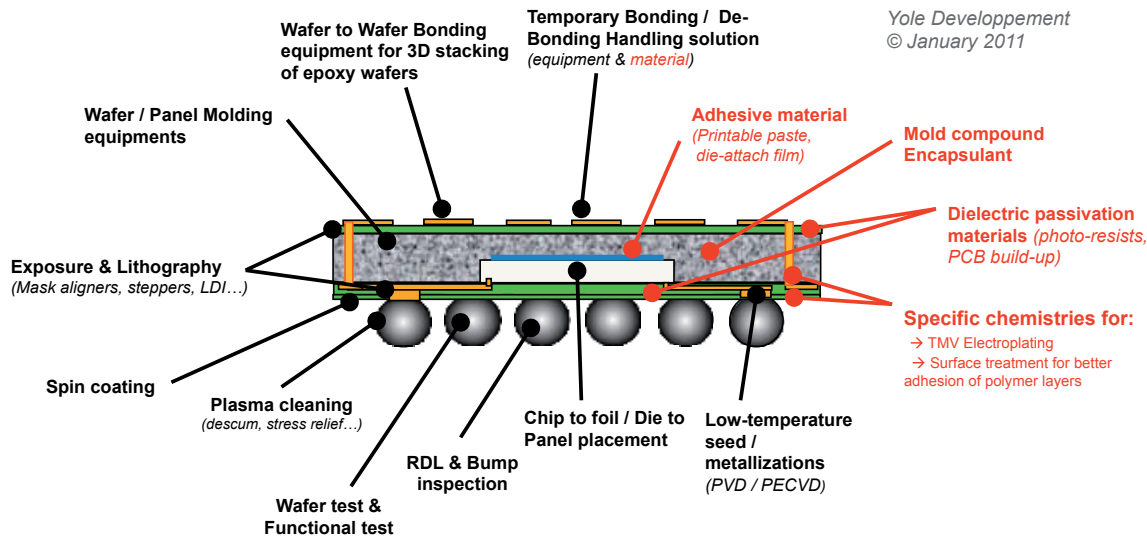
Not surprisingly, materials are viewed as an area with great potential for breakthroughs. "Users are tired of upgrading equipment with each new generation of products," says Lerner. "Material scientists have the opportunity to create scalable materials that can serve the



More and more key back-end realizations are happening at the wafer-level (Courtesy of Novellus)

## Equipment & Materials Tool-Box for 2<sup>nd</sup> generation FO WLP manufacturing

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Extracted from Yole Développement's 2011 report on "Equipment & Materials for the Wafer-Level-Packages"

industry through several generations of design, on the same equipment platform. This adds value to the industry in terms of both cost and environmental impact."

New materials are under investigation for TSVs, notes Srinivas. "However, copper electroplating appears to be the front-runner for the fill, and PVD seems to be the process of choice for barrier/seed, both of which are already production proven for front-end applications, and which together tackle several of the known TSV integration issues such as thermomechanical robustness," he adds.

From Davis and Chung's perspective, examples of 'mid-end' materials on the horizon that require further development involve barrier materials such as ultrathin barrier layers and thermally stable organic self-assembled barrier materials. They also believe that interlayer dielectric materials such as ultralow-k materials and air gaps need work. And for interconnect conducting materials they expect to see novel polymers, carbon nanotubes, graphene, and nanosolders emerge. For encapsulation materials, they say that desirable qualities include: low CTE, low modulus, high electrical resistivity, high thermal conductivity, high moisture resistance, and high adhesion to materials.

Henkel Electronic Materials LLC is also focusing on several areas for the 'mid-end,' including advanced underfill solutions for TSVs and other advanced flip chip packages or bumped dies, according to **Kevin Becker**, Henkel's director of technology. "This includes all kinds of pre-applied underfills, nonconductive pastes, nonconductive films, and wafer-applied underfill," he says.

One of the biggest challenges Becker sees is that the overall assembly process flow has yet to be

determined; it isn't standardized or even determined yet. "For materials pre-applied to the wafer, this is a huge challenge for us. At what point it's applied and what processing is done to the wafer after our material is applied really determines the material requirements," he explains. "Process dictates material properties. For example, the composition of the bond pads on either side of the substrate or on top of the bottom die in the stack will have a big impact on the material properties required for the underfill, whether it needs to be fluxing, how quickly it needs to cure. The bonding process will also dictate that, whether they're going to use thermal compression bonding, gravity reflow, ultrasonic, or something else."

Henkel is heavily involved with materials for FOWLPs, such as Infineon's embedded wafer-level ball grid array (eWLB) technology. "Compression molding is being used to make 'virtual' wafers, reconstituted wafers, which is a new process to the market," explains Becker. "A lot of work is done on these molded wafers. It's a somewhat immature technology; it's changing very quickly, so the requirements for compression molding materials are also changing. The key challenge here, whether it's a substrateless package, compression molding for chip-on-wafer, or other package types, is to manage the warpage. Molding a 12-inch ultrathin wafer that's asymmetric and getting near zero warpage to enable a dicing process, redistribution process, or stacking process, is the biggest challenge for that particular type of package."

And yes, Becker sees materials that still need to be developed for 3DICs. He cites underfills, nanofillers, and backgrinding as being technologies that aren't quite ready yet. "There are many temporary bonding requirements for TSV packages, particularly to enable mounting of the wafer for various processing, then

easy release afterward," he says. "I'm sure there are other issues as well, but the underfill solution and all of the various temporary bonding adhesives for backgrinding through dicing and other wafer-level processing still aren't there yet."

As far as where materials are heading, Becker believes that graphene certainly has great properties and won't be surprised to see big innovations come out of the technology within the next 3 to 5 years. He also expects innovations in cure latency and nanomaterials. Thermal conductivity is another big issue in 3DICs, particularly if there's any power or logic involved, so he hopes to see big innovations in these and other areas as well.

### Standardization

Many in the industry had hoped to see more processes standardized by now.

There are many reasons for the delay, but as Bair notes: One is that industry goals, such as those for TSV diameter, were initially in terms of 15, 20, 25µm, but R&D groups moved ahead very aggressively to shrink them to 10µm or smaller. In doing so, standardization was delayed. "But it brings the advantages of 3D to products much sooner, because the smaller vias have less impact on the die area. In terms of thin wafer handling and temporary bonding, there wasn't an expectation that standardization would occur by now; it's still a work in progress," he explains.

But with all of the announcements about bringing 3DICs to market lately, the lack of standardization in terms of equipment and processes at this point is surprising. "It seems like there should be more maturity in the infrastructure," says Becker.

Everyone seems to agree that standardization is still a ways out. "We still have a long way to go in regard to standardized processes. The 3D pioneers use a wide variety of integration concepts, process flows, equipment configurations, processes, and materials. SEMI recently formed a 3DS-IC standards committee, with task forces for bonded wafer stacks, inspection and metrology, and thin wafer handling," Matthias says.

Garrou believes that when major players such as TSMC and Samsung, who are in process qualification with their major customers right now, are finished and release their ground rules, it will generate the materials requirements the industry is searching for in terms of standardization.

### Consolidation ahead

Consolidation is common in semiconductor equipment companies and we've already seen some evidence of this in the 3DIC arena, namely Applied Materials' acquisition of Semitool at the end of 2009.

Some established companies have the size and infrastructure to support big customers. When new technologies come up, it may not always come from those large established companies, so they buy the technology and try to force consolidation.

"Another reason behind consolidation is frequently pressure from markets. For any major investment into equipment, customers want to ensure that the supplier has the short-term and long-term capability to support the installed base and can also ramp the production volumes quickly enough," explains Bair. "And if you take a look at the number of foundries able to process new technology, it's constantly shrinking—and they tend to want large equipment companies to work with and support them."

### Sally Cole Johnson for Yole Développement



**Thorsten Matthias** is director of business development at EV Group headquarters in St. Florian, Austria. In this role he is responsible for overseeing EVG's worldwide business development.

Matthias received his PhD in technical physics in 2002 from Vienna University of Technology. In his current role, he works in 3D integration, MEMS, LED, and nanotechnology.



**Steve Lerner** is CEO of Alchimer SA, and a 30-year semiconductor industry veteran, most notably fostering emerging technologies in first level interconnects. He has held executive positions at start-ups Alpha Szenszor, GigaSys, CS2, and contractors Amkor, Swire, and IMI.



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in 3D technologies and applications, he is focusing on SUSS' 3D packaging and 3D integration product portfolio. Bair is also the general manager of SUSS' US organization.



**Mark Davis** is a product manager for packaging materials at JSR Micro. He has 20 years' experience in the semiconductor industry in field applications engineering, sales, marketing, and product management.



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global director of technology and new business development and new business development for Dow Chemical's Electronic Business Unit. He is a fellow of both IEEE and IMAPS, and has served as president of the IEEE CPMT (2003-2005) and IMAPS (1997).



**James Chung** is a program manager in emerging technologies at JSR Micro. He holds a BS in chemical engineering from the University of Illinois at Urbana-Champaign and a PhD in physical chemistry from UCLA. Chung has worked at Intel

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**Kevin Becker** is director of technology at Henkel Electronic Materials, LLC, and heads the Advanced Materials Group as well as the Film Adhesives Development Group. He joined Henkel in 1999

and has been responsible for developing and launching several new product lines. Most recently he has overseen Henkel's launch of the new non-conductive paste pre-applied underfill for fine-pitch copper-pillar-based applications processors.

**Arthur Keigler** is chief technology officer, vice president of advanced technology at NEXX Systems. He has more than 20 years' experience in wafer processing, and holds an MS in materials science and engineering from MIT, as well as a BS in applied and engineering physics from Cornell. Keigler was also a Leaders for Manufacturing Fellow at MIT, earning an MS in mechanical engineering. He holds several patents in the field of wafer processing equipment.