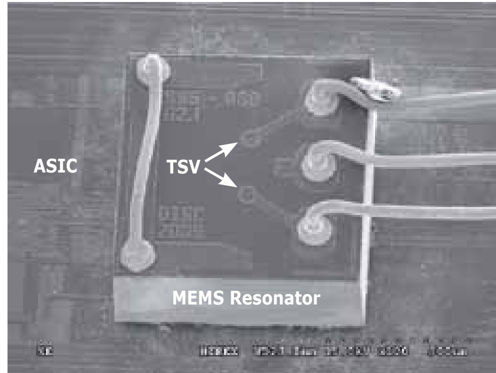
WHAT'S INSIDE?

Silex TSV in MEMS oscillator from Discera

The Discera DSC8002 is a programmable CMOS oscillator incorporating a Silicon MEMS resonator.

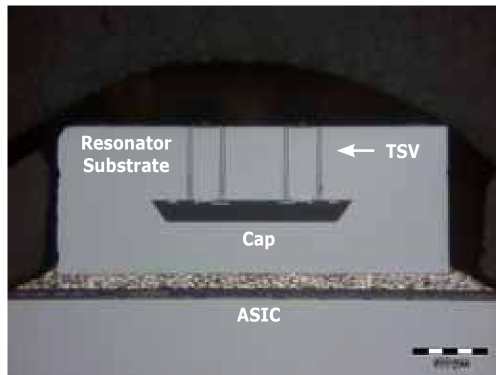
It is provided in several packages, the smallest being a 4-pin MLF whose dimensions are 2.5x2x0.85mm. Thanks to a Silicon Fusion Bonding process and TSV connections the resonator achieve an area of only 0.27mm²



Resonator die – SEM Tilt View (Courtesy of System Plus Consulting)

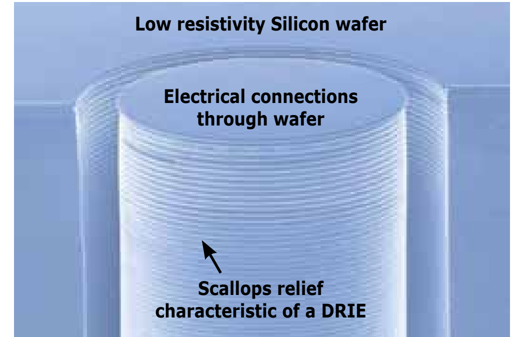
Technology analysis

The manufacturing of the resonator is realized by Silex Microsystems probably on 6-inch wafers. The MEMS resonator is wafer-level packaged and electrical connections are realized by TSV.

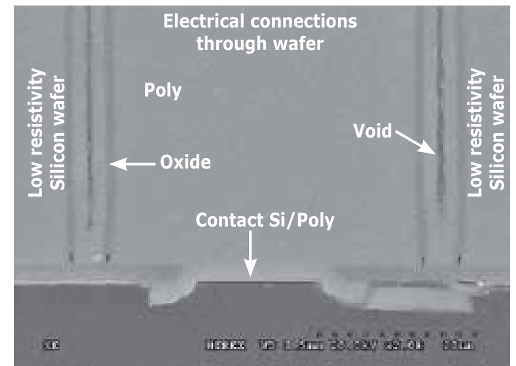


MEMS Resonator Cross-Section (Courtesy of System Plus Consulting)

"The MEMS resonator die size has been shrinked by almost 4 times," explains Romain Fraux, System Plus Consulting



Annular TSV without filling (courtesy of Silex)

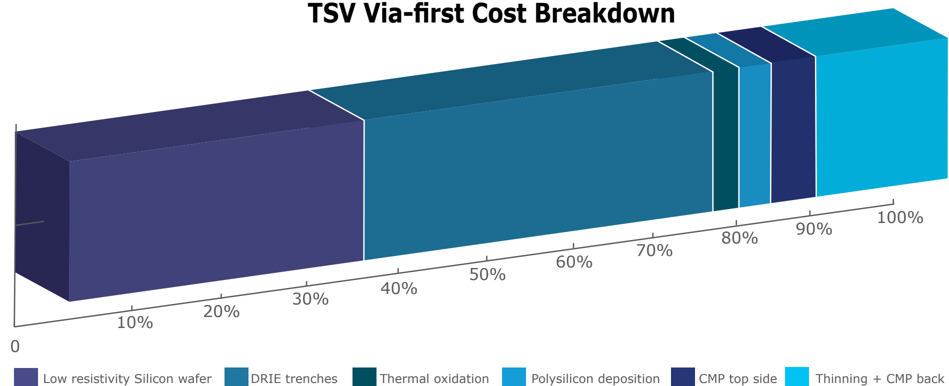


TSV Details – SEM View (Courtesy of System Plus Consulting)

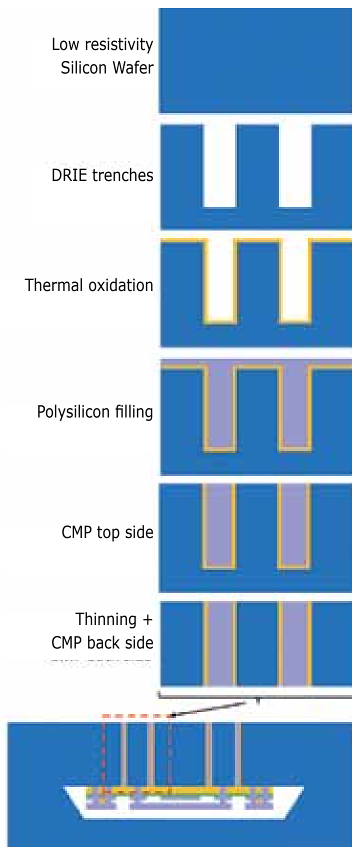
The TSV are realized with the Silex TSI™ technology: through-wafer trenches are created by DRIE and filled with an isolating dielectric. The TSI™ technology is applied to a highly doped Si wafer, a closed vertical trench around a "plug" of Si constitutes an isolated electrical connection through the wafer (through silicon via – TSV).

TSV Via-first process flow

The TSV are realized on the low resistivity silicon wafer of the resonator prior to the manufacturing of the resonator itself. First, the wafer is patterned and TSV are etched by DRIE. In order to keep the via plug in position, the trench etch stops short of reaching all the way through the wafer (the final trenches have a



(Courtesy of System Plus Consulting)



TSV Via-First process Flow
(Courtesy of System Plus Consulting)

depth of ~100µm). Then the trenches are filled with the isolating dielectric: a thermal oxide is grown on the wafer followed by a deposition of polysilicon which fills the via. The layers of oxide and polysilicon are removed from the surface of the wafer by CMP. Finally, a thinning process (backgrinding + CMP) is applied to the backside of the wafer, removing the material that keeps the "via plugs" connected to the bulk, thereby isolating the via plugs from the bulk of the wafer.

Cost analysis

TSV induces an additional cost to the front-end process and represent ~17% of the manufacturing cost of the final wafer. The saving in silicon area due to TSV connections is hardly calculable, but in addition with the silicon fusion bonding process the MEMS resonator die size has been shrinked by almost x4 compared with the first generation of Discera MEMS resonator.

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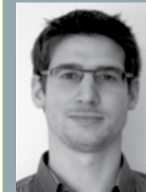

Romain Fraux, Electronics Cost Engineer, System Plus Consulting

Romain Fraux is Project Manager for Reverse Costing analyses at System Plus Consulting. Since 2006, Romain is in charge of costing analyses of MEMS devices, Integrated Circuit and electronics boards. He has significant experience in the modeling of the manufacturing costs of electronics components.
Romain has a BEng from Heriot-Watt University of Edinburgh, Scotland and a master's degree in Microelectronics from the University of Nantes, France.

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